CONTENTS

CHAPTER 1
INTRODUCTION

CHAPTER 2
INTERFACE CONSIDERATIONS

CHAPTER 3
SYSTEM DESCRIPTION

CHAPTER 4
OPERATION AND PROGRAMMING INFORMATION

CONTENTS (Cont.)

ILLUSTRATIONS

TABLES

Type 339 Programmed Buffered Display

Type 339 Buffered Display System

CHAPTER 1
INTRODUCTION

The Type 339 Programmed Buffered Display (Frontispiece) is an on-line system manufactured by Digital Equipment Corporation for operator observation, manipulation, and alteration of computer-stored data. The display system consists of a precision incremental CRT display, display control logic, light pen, pushbutton control box, and interface logic for communication with a PDP-9 computer. The computer processor and the display control logic share the computer memory, and are interdependent as a system.

The computer system furnishes rapid data storage and retrieval for display as dots, lines, curves, or characters (optional) on the face of the CRT. The operator can manipulate or alter the data by using the light pen, pushbutton control box, or the keys and switches on the computer console.

1.1 PHYSICAL DESCRIPTION

The Type 339 system is housed in two standard DEC cabinets bolted together. The cabinets contain the CRT associated circuits and the display logic. Additionally one Type 1943D rack of modules comprising the interface logic is installed in the mainframe of the PDP-9 computer.

The display system weighs 900 lb. The dual cabinet measures 69-1/8 in. high, 42 in. wide, and 51 in. deep. When installed the system must have a 2-ft clearance at all access doors and at the sides of the equipment. A minimum clearance of 3 ft is required for removal of the CRT assembly.

1.2 EQUIPMENT SUPPLIED

Table 1-1 lists the components of the Type 339 Display System and Figure 1-1 shows the component locations in the dual cabinet.

Table 1-1
Type 339 Equipment Supplied

Type	Nomenclature	Quantity
16ADP7A	CRT Display	1
DEC	Deflection Amplifiers	1
DEC	Control Logic	1
DEC	Control Box	1
DEC	Indicator Panel	1

Table 1-1 (cont)
Type 339 Equipment Supplied

Type	Nomenclature	Quantity
DEC 370	Light Pen	1
DEC VL09	Interface Logic	1
DEC 770 (10 kV)	Power Supply	1
DEC 734B	Power Supply	1
DEC 728	Power Supply	4
Trygon (50V)	Power Supply	1
DEC 832D	Power Control	1
DEC 836	Power Control	1
	Options (see Page 1-5)	

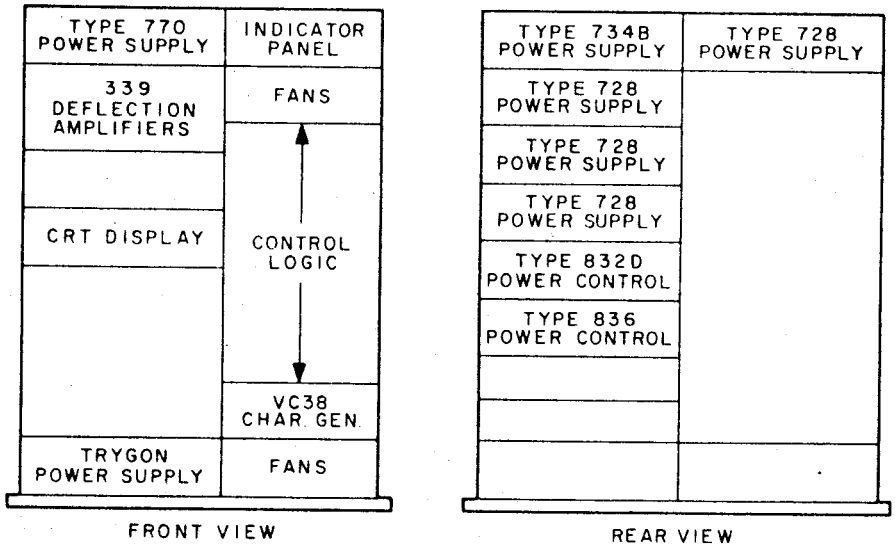


Figure 1-1 Type 339 Display System, Component Locations

1.3 FUNCTIONAL DESCRIPTION

The Type 339 Display is a dual processor system in that the display and its associated PDP-9 computer both have processors which operate the computer memory. The only difference is that the display processor (display control logic) can read information only from memory, but the computer processor can read and write. Using the pushbutton control box, light pen, and computer teletype (optional character mode), the operator can communicate directly with the computer and observe the results of his interaction on the display. These display peripherals are connected to the I/O bus and the display. The

display processor is controlled from the I/O bus, but receives its commands and data via the direct memory access (DMA) channel. Associated instructions (display commands and IOT instructions) are stored in memory. The display file words are loaded into a table or block of successive memory locations; the beginning address of this table is loaded into a special register called the display address counter (DAC) and allied break field register (BF). The contents of these registers are applied to the inputs of the computer memory address register (MA), forming a 15-bit address which can increment across memory field boundaries for access to a total of 32K of memory. A DMA break is then initiated by either the display or the computer, and the address is read into the MA. The computer then goes into the single DMA break cycle in which it fetches the word from memory and transfers it from the memory buffer register (MB) to a buffer register (DX or DY) in the display logic. During this time the display starts its operation and the DAC is incremented by 1. The computer program counter (PC) is not incremented during the DMA cycle. At the end of the DMA cycle the computer continues its main program until the display requires another DMA break.

1.3.1 Display Modes

Three groups of IOT instructions permit two-way communication and interaction between the computer and the display. The first group reads the status of various display registers into the computer AC register. The second group transfers initializing command information from the computer to the display, and the third group allows the computer to test registers in the display and perform instruction skips if certain conditions are met. Among the prestored command words, a mode command initializes the display to operate in one of seven available modes:

Point Mode:	Positions the electron beam at the point specified by x and y coordinates
Increment Mode	Moves the beam from its initial position to any point up to 3 bits away in any of eight directions
Vector Mode	Displays a line between the initial position and a final position which is located relative to the initial position by DX and DY increments. (The line may be invisible, i.e., not intensified.)
Vector-Continue Mode	Similar to vector mode, except that line is extended through final position to edge of usable picture area.
Short Vector Mode	Same as vector mode but DX and DY packed in one word.
Graph-Plot Mode	Automatically increments one coordinate while accepting values for the other to plot a function of an "independent variable."

Character Mode (Optional) — Displays ASCII characters specified by 6- or 7-bit code. Two versions are as follows.

a. Software - Points comprising each character are stored as subroutines in computer.

b. Hardware - Points are stored in read-only memory in display.

1.3.2 Timing

After the display has been initialized and started with the IOT instructions, it requires information at a high transfer rate in order to visibly draw the picture. The DMA channel provides the information at the required speed. The display timing has been set so that it can request one DMA break cycle out of five machine cycles, preventing the display from taking too much time from the computer. This amounts to a DMA break at a maximum rate of once every 6 μs. In most cases, the display requires more than 6 μs to process the information, and thereafter obtains a break when more information is needed. The computer transfers only 12 bits of information at a time to the display. Other high-speed equipment can be used at the same time as the display, by incorporating the optional DMA multiplexer DM09A in the channel so that up to three high-speed devices, including the display, are gated onto the channel one at a time.

1.3.3 CRT Display

The CRT Display is a 16-inch tube with 9-3/8 in. by 9-3/8 in. usable display area. Magnetic deflection and focusing techniques result in uniform resolution over this area, described by 1024 bits in both the X and Y directions, providing approximately 0.01 in. per bit. The X and Y position registers in the display logic are 13-bit registers which can describe 8192 bits in both directions or a 75 in. by 75 in. page. Information can be displayed anywhere on this page through a technique called scissoring which allows the 9-3/8 in. by 9-3/8 in. screen or "window" to be moved anywhere on the page. Information can be viewed only through this window. The picture being displayed must be in other than point mode and must be a closed loop figure, i.e., after finishing a picture, a vector is drawn back to the origin. If it is desired to move the picture up, a short vector is drawn before drawing the picture. The effect of this vector is cumulative and, if it is within the closed loop, it will add each time the display cycles through the file. Pushbuttons are usually used to determine the direction of movement.

Up to seven display CRTs may be remotely slaved to the master CRT, and all can receive identical information, different information, or a combination can be established. The routing of information to a slave display is a function of display file commands.

1.4 OPTIONS

1.4.1 Character Generator VC38

This option provides the capability for displaying characters on the scope face. The characters are stored in PDP-9 memory as subroutines; the VC38 consists of additional hardware required to dispatch to the subroutines. Average character display time is 50 μs. If 6-bit character codes are used, they are packed two per 18-bit word; if 7-bit character codes are used, packing is one per word (both versions are right-justified).

1.4.2 Character Generator VA38

The VA38 allows the 339 to display one of a standard character set from a read-only memory located in the display. As the character data are in hardware, one character display time is 20 μs; programming is simplified to a Mode command, followed by 6- or 7-bit character codes.

1.4.3 Slave Option VS38

The slave option provides interface, control, and driving circuits that allow up to eight CRT displays, including the master, to use the 339 graphic capabilities. Eight different, identical, or combinations of pictures are possible. The master CRT can be treated as a slave. If not, all pictures sent to all slave units are superimposed on the master CRT.

1.4.4 Search Option VF38

With the addition of the VF38 Search Option, the display file can be searched for a series of vectors or increment words. This option provides circuits for stopping the display control logic if a display instruction in a selected mode is about to be executed. The selectable modes are increment mode and the three vector modes. After the display stops, a flag informs the computer program that the search logic has found a word of interest. A computer instruction causes the display to execute the instruction that caused the flag, and to proceed to the next display instruction.

1.4.5 Zoom Option VZ38

The X and Y registers of the 339 contain 13 bits each. Normally the low-order 10 bits of both are gated to the CRT deflection circuits. Through a manual switch, the zoom option allows the gating of the 10 high-order bits instead of the 10 low-order bits.

1.4.6 Track Balls

Track balls permit the operator to move a mechanical device and cause the picture to rotate in the same direction as the device. The option contains registers which count the movements of the track ball in the X, Y, and Z directions. These registers are read by the computer and implemented in the display file.

1.4.7 Tablets

Tablets consist of a resistive surface from which the X and Y position of a metallic pen can be determined. These positions are temporarily stored in registers and later used by the computer to draw pictures or position objects on the tube.

1.5 REFERENCE DOCUMENTS

Table 1-2 lists the major documents supporting the 339 Display System.

1.6 SPECIFICATIONS

Table 1-3 summarizes the properties of the 339 Display System.

Table 1-2
Type 339 Reference Documents

Title	Document Number	Description
PDP-9 User Handbook	F-95	Operation and Programming of PDP-9
PDP-9 Maintenance Manual	F-97	Operation and Maintenance of PDP-9
Instruction Manual 338 Programmed Buffered Display	DEC-08-H6AA-D	Operation and Maintenance of 338 Display (338 plus VL09 equals 339 Display System)
339 Programming Manual		Programming of 339
Instruction Manual Light Pen 370	H-370	Operation and Maintenance of 370 Light Pen

Table 1-2 (cont.)
Type 339 Reference Documents

Title	Document Number	Description
KF09A Instruction Manual	DEC-09-I5AA-D	Operation and Maintenance of PDP-9 Automatic Priority Interrupt (API) option
DM09A Instruction Manual	DEC-09-I9AB-D	Operation and Maintenance of PDP-9 DMA Multiplexer option
KG09B Instruction Manual	DEC-09-I1AB-D	Operation and Maintenance of PDP-9 Memory Extension Control option
Logic Handbook	C-105	Standard FLIP CHIP Modules and products used in the 339

Table 1-3
Type 339 Performance Characteristics

Function	Capability
Operating temperature	50 to 110°F
Operating humidity	0 to 90% relative humidity
Storage temperature	32 to 122°F
Storage humidity	Less than 90%
Input power	115 ± 10V, 60-c/s single phase
Power and heat dissipation	1.5 kW, 4950 Btu/hr
Ambient temperature	50°F (10°C) to 110°F (43°C)
Cathode ray tube	16ADP7A. Radius of curvature 50 in.
Raster size	9-3/8 in. by 9-3/8 in. containing 1024 points by 1024 points
Pincushion distortion	Less than 3/32 in. per side
Deflection and focus	Magnetic
Spot size	Approximately 0.030 in., 0.015 in. at the half-light output points
Address scheme	2's complement, with (0,0) located at the lower left-hand corner of the raster
Stability	±0.05 in. in 8 hr at a nearly constant temperature (±3°F)
Repeatability	±0.05 in. regardless of the location of the previous spot
Timing	6.0 μs for information transfer, 35 μs per point for random positioning, 1.1 μs per point in the vector, vector continue, increment and character modes

Table 1-3 (cont.)
Type 339 Performance Characteristics

Function	Capability
Modes	Point, increment, vector, vector continue, short vector, graph plot, character (2)
Intensification	Preset at 0.3 μs per point
Indicators	The current state of the coordinate registers and all other major functions is shown by indicator lights at the top of the right-hand bay (see Figure 1-1).

NOTE

For the Type 370 light pen, the light pipe minimum bend radius is 3/4 in.

CHAPTER 2
INTERFACE CONSIDERATIONS

2.1 COMPUTER I/O SYSTEM

The display, the computer, and their peripheral equipment communicate through the I/O bus and the DMA channel. The I/O bus is used to service relatively slow devices which do not require a high information transfer rate. The DMA channel enables peripheral devices including the display system to directly access memory in a matter of microseconds. Devices using the channel are controlled by IOT instructions via the I/O bus.

Figure 2-1 shows the interconnection between the peripheral equipment and the computer. If more than one peripheral is on the DMA channel, a DM09A Multiplexer must be used to transfer the data to the proper peripheral (up to three peripherals per DM09A).

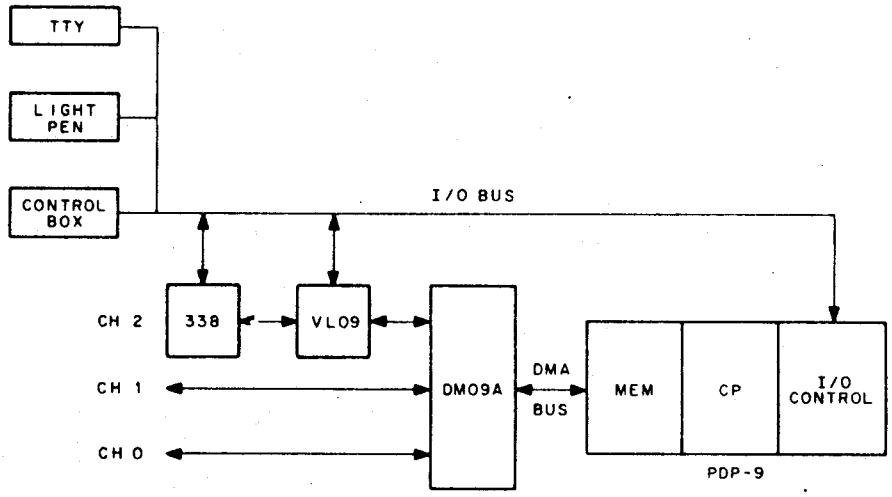


Figure 2-1 Display Interface

Using the control box, light pen, and PDP-9 teletype, the display operator can communicate directly with the computer and observe his interaction on the display. These devices are connected via the I/O bus to the PDP-9 program interrupt (PI) facility and/or the optional automatic priority interrupt (API) system to enter servicing subroutines. These subroutines are normally used to alter the existing display program in memory, whereas the actual transfer of command and data from memory to the display is performed during the DMA break cycles.

2.1.1 Program Interrupt Facility

The PI feature of the PDP-9 allows the display to initiate an interrupt of the main program. This releases the main program from the necessity of making repeated flag checks. The PI feature has the lowest priority in the PDP-9 program break hierarchy. Essentially, a program interrupt causes the computer to interrupt its current program operation, store the contents of key registers in assigned memory location 00000, and branch control from location 00001 to a subroutine servicing the I/O device that requested the interrupt. In the 339 display system, any of the following display flags can set the display interrupt flag to cause a program interrupt if the interrupt system is enabled:

Internal Stop
External Stop
Light Pen Hit
Edge Violation
Pushbutton Hit
Manual Interrupt

2.1.2 Automatic Priority Interrupt Option

The flags listed above may also be connected to the API option if a higher interrupt priority is desired. The API provides four hardware priority levels above the PI priority, and the peripheral flags associated with the display system are normally assigned to API priority level 2 of the four descending order priorities 0, 1, 2, 3.

2.1.3 DMA Channel

The DMA break facility allows the display system to obtain direct access to the PDP-9 memory. This facility has highest priority in the PDP-9 program break hierarchy. Sequencing of the DMA break function begins with a break request from the 339 display to the PDP-9 central processor. The direction of data flow is determined in the I/O control section of the computer. The DMA break facility controls entry into the break cycle, generates the necessary control signals to gate address and data into the MA and MB registers respectively of the computer during data input operations, and specifies when data is ready for the display during output operations.

2.1.4 I/O Skip Facility

The PDP-9 I/O facility is used to check the device status flags under program controlled IOT instructions. This facility permits the program to skip the next sequential instruction, allowing exit to a subroutine for servicing the display.

2.2 VL09/DM09A/PDP-9 INTERFACE

The VL09 is one rack of logic that is designed to interface between the 338 display and the PDP-9 computer. It uses FLIP CHIP modules of the R, B, and W series and is mounted in the mainframe of the PDP-9. A 339 consists of a VL09 and a 338.

2.2.1 Interconnection

The VL09 is interconnected as shown in Figure 2-2, using the following cable configurations:

Thirteen 15-ft coaxial cables from the 339 to the VL09

Two variable-length I/O bus cables from the PDP-9 to the VL09

Seven 10-ft flexprint cables from the DM09A to the VL09

The DM09A connections shown in Figure 2-2 are for DMA channel 2. In instances where the VL09 is to be inserted in a channel other than 2 (0 or 1), the correct cable slots can be found by referring to the DM09A cable diagrams.

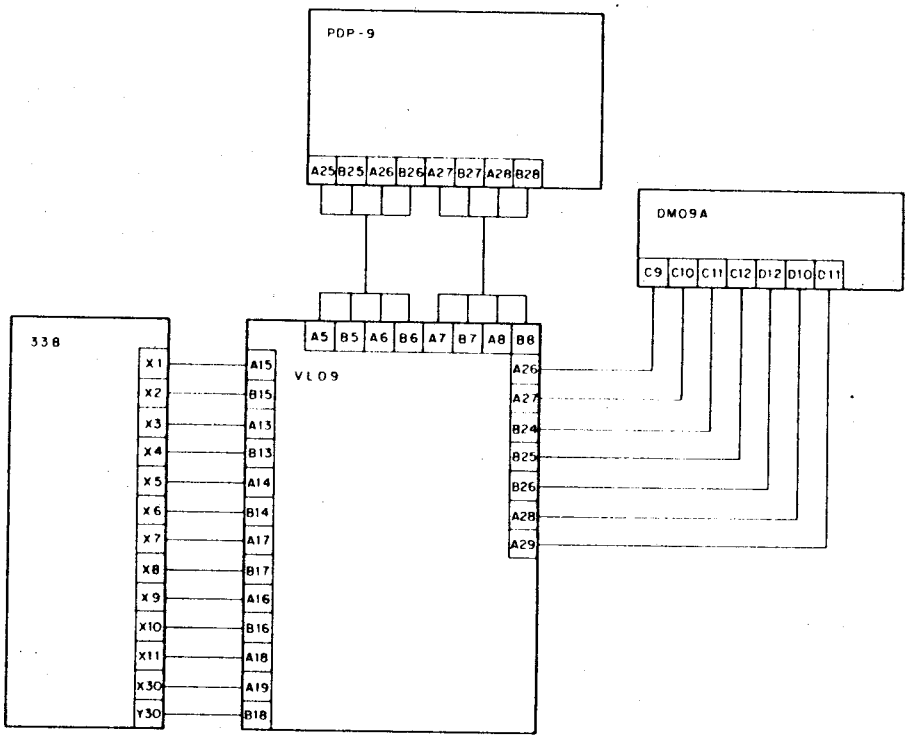


Figure 2-2 Interface Cabling

2.2.2 Power Requirements

The VL09 requires the standard FLIP CHIP voltages of +10, -15, and ground. A separate supply is not needed since the VL09 has less than 20 modules. The power comes from the PDP-9.

2.2.3 VL09 Specifications

The function of the VL09 is to provide the proper polarity signals to the PDP-9 and the display. In cases where the signals are of the desired polarity, the VL09 either buffers the signal or sends it to its destination.

2.2.4 Signal Description

Figure 2-3 shows the signal lines between the display, VL09, DM09A, and the PDP-9 I/O bus. Brief descriptions for these signals follow.

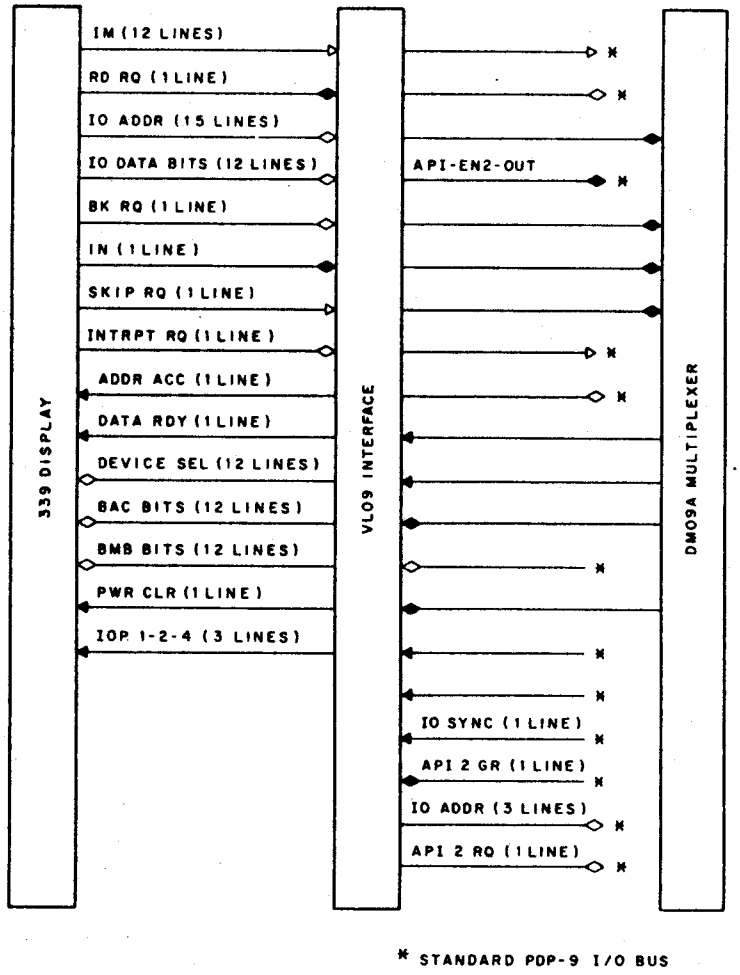


Figure 2-3 Interface Signals

2.2.4.1 IM Lines - Twleve input mixer lines (IM) originate in the 338 and travel to the VL09 via a 15-ft coaxial cable. From the VL09, the IM lines are sent to the PDP-9 on the I/O bus.

2.2.4.2 I/O Address Lines - Fifteen I/O address lines originate in the 338 and travel to the VL09 via coaxial cable. These lines must be inverted from ground to -3V because the DM09A requires negative levels for assertion. The I/O address lines are sent to the DM09A via 10-ft flexprint cabling.

2.2.4.3 I/O Data Bits - The I/O data bits (12) are handled in the same manner as the 15 I/O address lines.

2.2.4.4 RD RQ Line - The read request line originates in the 338 and is sent to the VL09 via the 15-ft coaxial cabling. The VL09 inverts the negative level to a positive level and sends it to the PDP-9 via the I/O bus. The PDP-9 requires a 1-μs positive pulse to read information into its accumulator. When any of the following Read Status commands are given, the RD RQ line will go to ground.

RPDP - 700501	RS4 - 700602	RCG - 701662
RXP - 700502	RSG1 - 700622	RS1 - 700602
RYP - 701602	RS5 - 701642	RS2 - 701622
RDAC - 700601	RSG2 - 701642	RS3 - 701621
		RPB - 700521

2.2.4.5 BK RQ Line - The break request line originates in the 338 and is sent to the VL09 via the 15-ft coaxial cabling. The VL09 inverts the positive level to a negative level and sends it to the DM09A via the 10-ft flexprint cabling. The BK RQ line tells the PDP-9 that a request for input or output data has been made by the 338. The BK RQ line forces the PDP-9 to go into a DMA break cycle following completion of the current program execute cycle.

2.2.4.6 IN Line - The IN line originates in the 338 and travels to the VL09 via the 15-ft coaxial cabling. The signal is then sent to the DM09A via the flexprint cabling. If the signal is at -3V, data goes into the PDP-9. If the signal is at ground, data goes from the PDP-9 to the display.

2.2.4.7 Skip RQ Line - The skip request line originates in the 338 and travels to the VL09 via the 15-ft coaxial cabling. The VL09 sends the positive pulse to the PDP-9 via the I/O bus.

2.2.4.8 INT RQ Line - The interrupt request line originates in the 338 and travels to the VL09 via the 15-ft coaxial cabling. The positive INT RQ line is ANDed with a REQ signal that is generated in the

W104 module. The W104 module sends a PROG INT RQ as well as an API RQ to the PDP-9 via the I/O bus. Either signal will interrupt the program, depending on which interrupt system is enabled.

2.2.4.9 ADDR ACC Line - The address accepted line originates in the DM09A Multiplexer and travels to the VL09 via the flexprint cabling. The ADDR ACC pulse is buffered and sent to the 338 display. It clears the BK RQ flip-flop and the DX register.

2.2.4.10 DATA RDY Line - The DATA ready line originates in the DM09A and travels to the VL09 via the flexprint cabling. The negative pulse is buffered and sent to the 338 display. It triggers the DATA STROBE and DATA STROBE +0.5 pulses.

2.2.4.11 DEVICE SEL Lines - Eight device select lines originate in the PDP-9 as negative levels. They are inverted in the VL09, and both polarities are sent to the 338 display. The device select bits generate the I/O code for specific devices.

2.2.4.12 BAC Bits - The buffered AC lines originate in the PDP-9 as ground levels. They are presented to the VL09 via the I/O bus.

2.2.4.13 BMB Bits - The buffered MB bits originate in the DM09A and travel to the VL09 as negative levels. The lines are called AM bits in the DM09A. The VL09 inverts the levels and sends them to the 338.

2.2.4.14 PWR CLR Line - The power clear line originates in the PDP-9 (I/O RESET). It is buffered in the VL09 and then sent to the 338 display.

2.2.4.15 IOP1/2/4 Lines - The input-output pulses 1, 2, and 4 originate in the PDP-9 and are buffered before being sent to the 338 display. These pulses strobe the W103 modules, which produce the IOT pulses in the 338.

2.2.4.16 API EN 2 OUT Line - The automatic priority interrupt enable out line originates in the VL09. If the 338 is not asking for an API, the line is at -3V. The API EN 2 OUT line goes to the next device down the line via the I/O bus as an enable level. If the 338 is asking for an API, the level goes to ground and the next device down the line is inhibited from asking for an API.

2.2.4.17 I/O SYNC Line - The I/O sync pulse is generated in the PDP-9 and travels to the VL09 via the 15-ft coaxial cabling. It strobes the API 2 RQ line to a 1.

2.2.4.18 API 2 GR - The automatic priority interrupt grant line is a negative level generated in the PDP-9 that tells the device whether its API request has been answered.

2.2.4.19 I/O ADDR Lines - Three I/O address lines are generated by the W104 module in the VL09. If an API request has been granted, the display interrupts to a specific location in memory (00054).

2.2.4.20 API 2 RQ Line - The automatic priority interrupt 2 request line originates partially in both the 338 and the VL09. The interrupt level comes from the 338 and is ANDed in the W104 of the VL09. The actual API 2 RQ comes from the W104 and goes to the PDP-9 I/O bus.

CHAPTER 3

SYSTEM DESCRIPTION

3.1 DISPLAY SYSTEM REGISTERS

The 339 Display System control logic contains several flip-flop registers as shown in Figure 3-1 and described below.

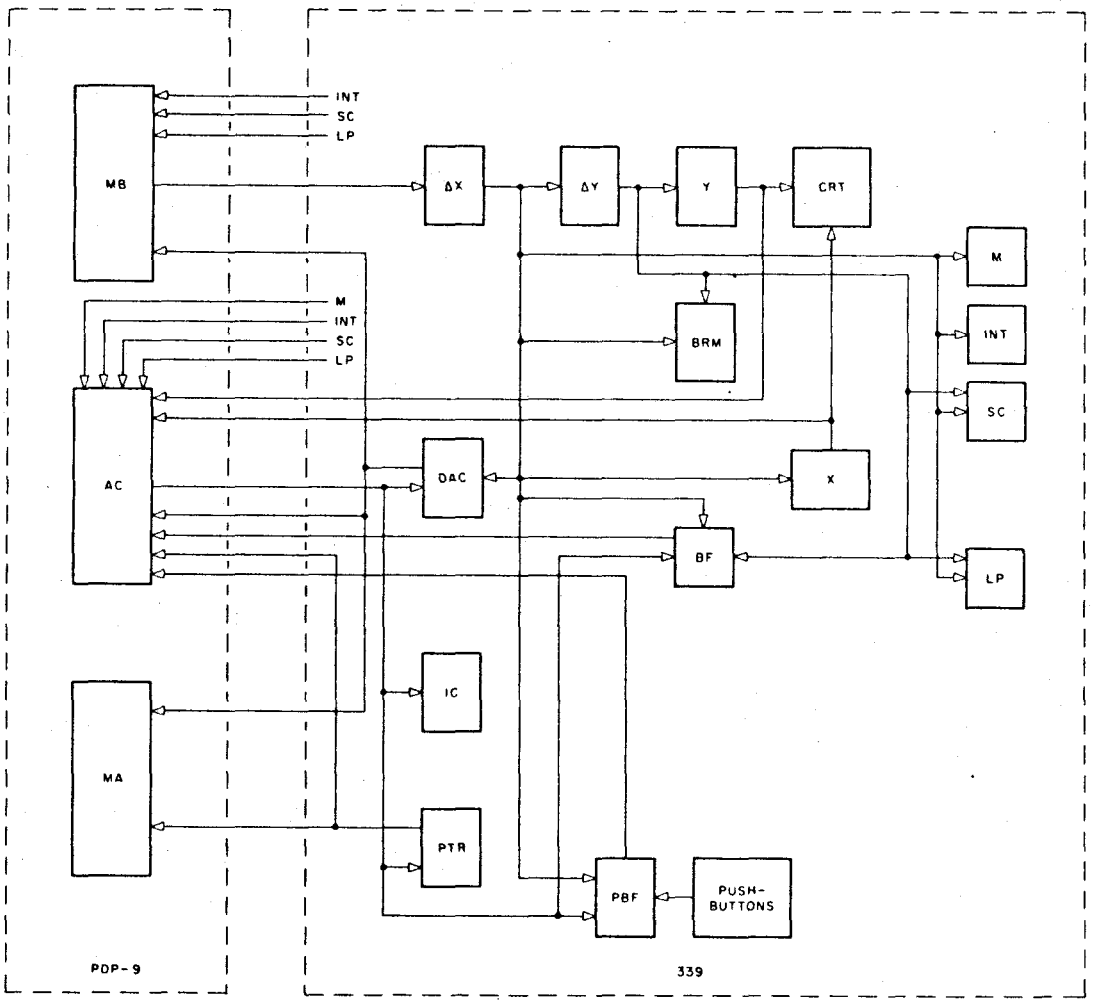


Figure 3-1 Type 339 Display, Registers

3.1.1 Display Address Counter (DAC)

The DAC is the primary address register in the display logic and is used with the PDP-9 DMA break system. It is a 12-bit counter (count up) and can be set from the PDP-9 accumulator (AC).

Associated with the DAC is a 3-bit break-field countup register, which allows the 339 system to address any of 32,768 words of core memory directly.

3.1.2 Delta-X Register and Delta-Y Register

The ΔX register is the main input register of the 339 control. It contains 12 bits and is not a counter. On a DMA break, a data word from the PDP-9 memory is transferred into the ΔX register. From there it is transferred to one or more of the other registers of the control.

During execution of many 339 instruction cycles, information in the ΔX register is transferred to the ΔY register, which is primarily a holding register. During a point-mode instruction, information from the ΔY register is sent to the Y-position register. Also, the ΔY register holds the ΔY component of vectors.

3.1.3 Pushdown Pointer (PDP)

The PTR serves as an address register during 339 subroutine instructions. It is a 12-bit up-down counter and can be set using an IOT instruction from the PDP-9 AC.

The subroutining structure of the 339 system uses the pushdown list which is located in the first 4192 words of the PDP-9 memory. During push-jump instructions, which obtain entry to subroutines, the 339 status is stored in one word of memory, and the return address from the subroutine is stored in the next word. If further push-jumps to deeper levels occur, the current status and return addresses are stored in consecutive pairs of words in memory, deepening the list.

Exits from subroutines are called POP instructions. During POP instructions, the PTR is counted down, and information is retrieved from the pushdown list, transmitted to the ΔX register, and from there sent to appropriate registers in the display control.

3.1.4 Initial Conditions Register (IC)

The initial conditions register is a 12-bit register that can be set by an IOT instruction from the PDP-9 AC. This register contains the information to set up the initial conditions of the 339 display control, such as enabling interrupts on special flags, setting the drawing size, enabling intensification, etc. The content of the IC register is not read back into the PDP-9 AC, nor is it transferred to any other 339 registers.

3.1.5 Mode Register

The mode register is a 3-bit register, which is decoded when data state is active to provide eight operating modes (one is a spare). The modes are point mode (000), increment mode (001), vector mode (010), vector-continue mode (011), short vector mode (100), VC38 character mode (101), graph-plot (110), and VA38 character mode (111).

3.1.6 Intensity (INT), Scale (SC), and Light-Pen (LP) Registers

The contents of the intensity register establish the level of picture brightness. The INT register has three bits. It may be counted up and down and can be set by control state instructions. The decoded three bits provide eight levels of intensification on the screen.

The contents of the scale register control consecutive dot spacing in the incremental drawing modes. The SC register is a 2-bit up-down counting register, which also can be set or counted by control state instructions.

The light-pen register contains three control flip-flops; LP enable, LP flag, and LP find. If LP enable is set to a 1 by control-state instructions, this allows an LP pulse to set the LP flag and LP find, provided that illumination is detected by the light pen.

3.1.7 X and Y Registers

The X and Y registers specify the current electron beam position. These registers are counted up and down in the incremental-drawing modes and are loaded directly from the ΔX and ΔY registers in point mode.

If the SC register contains 0, the X- and Y-position registers are counted only by 1 each step. If SC contains 1, they are counted by 2; if SC is 2, they are counted by 4; and if SC is 3 (maximum), the position registers are counted by 8.

3.1.8 Pushbutton Flip-Flop Register (PB)

The PB is a 12-bit register associated with the pushbutton control box. The PB can be set via an IOT instruction with information from the PDP-9 AC. It can also be read back into the AC. The contents of the PB are indicated on corresponding lighted buttons on the pushbutton control box.

To modify the PB contents the 12 buttons on the control box may be used to complement corresponding flip-flops in the register. To clear the PB, the control box has two clear pushbuttons, and each controls six flip-flops of the register.

3.1.9 Manual Interrupt Pushbutton

When the manual INTERRUPT pushbutton on the control box is depressed, it causes an interrupt request to be generated in the 339 logic. If the PDP-9 interrupt system is on at this time, an interrupt of the PDP-9 program occurs. Depressing this button does not stop the display.

3.1.10 Binary Rate Multiplier (BRM)

The BRM is a 10-bit up counter with a logic configuration designed to produce pulse trains. It is a major component in the vector-generating logic. During a vector sequence, the ΔY and ΔX registers are loaded with the vector information, and the BRM is counted from 0 through octal 1777 back to 0. The transition from all 1's back to 0 signifies the end of the vector.

3.2 CHARACTER GENERATOR REGISTERS (Contained in Option VC38)

These registers are associated with character generation:

Starting-address register (SAR)

Character-save register (CS)

Character-address counter (CHAC)

The character generator uses the dispatch-table technique for drawing characters; that is, a 6- or 7-bit character code represents the least significant bits (LSB) of an address. When this address is referenced in the PDP-9 memory, a word is transmitted to the display. This word may be the starting address in memory of the character itself, that is, the character represented by the 6- or 7-bit code, or it may be a control word, such as escape-from-character-mode, or a carriage return.

Characters are drawn in either the increment mode or the short-vector mode. Therefore, they can be any length and any shape, and are terminated by an escape from the increment, or short-vector, mode back to the character mode.

3.2.1 Starting-Address Register

This is a 6-bit register (not a counter) which is used with the character code to determine the initial reference in the dispatch table.

3.2.2 Character-Save Register

This 6-bit register holds the second character in a word. This is necessary because data transfers from the PDP-9 to 339 logic are in 12-bit words. When using 6-bit character codes, the leftmost

six bits of the computer word represent the first character, and the rightmost six bits of the computer word represent the second character. Thus, while the first character is being drawn, the second character code is saved in the CHSR.

3.2.3 Character-Address Counter

This 15-bit register is used precisely as DAC is used, except that it is limited to character generator operations. It is an up-counter and references consecutive addresses in core memory during execution of the characters.

3.3 PDP-9/339 DATA TRANSFERS

The PDP-9 registers affected by the DMA break system are the MB register and the MA register. A third register, the PDP-9 AC, is used with the I/O bus to load initial parameters into the 339 registers, and also to read PDP-9 status back into the AC under program control. The DMA-break logic is described in the PDP-9 Maintenance Manual.

During a break, one of the 339 address registers loads the MA register. The break system uses such address information to read a word from memory into the MB register for transfer into the 339 ΔX and IC registers. Only the ΔX and IC registers are loaded from the MB.

During a push-jump instruction, data from the 339 registers returns to the MB register to be stored in the pushdown list in memory. This information consists of light-pen status and scale, intensity, and mode information, the 3 bits from the break field counter, and the 12 bits from the DAC.

During a POP instruction, this status and return-address information is transferred from the MB into the ΔX register, from which it is returned to the break-field, DAC, light-pen status, scale, intensity, and mode registers.

3.3.1 Control-State Instructions

Chapter 4 describes data transfer between the 339 registers on an instruction-by-instruction basis. In control state, display instructions are executed in a manner similar to computer instructions. Each instruction has an OP code that determines the logic operations to be executed. These are either one- or two-word instructions and require from one to four break cycles for execution.

3.3.2 Data-State Instructions

The prime purpose of the data-state logic is to control the motion of the CRT beam. To do this, X- and Y-position registers are counted up and down. These registers are cleared and set for point-plotting instructions.

The display is always in control state at the start. To enter data state, a control-state instruction must first be executed. A parameter instruction with bit 17=1 or POP instruction with bit 17=1 causes the display to enter the data state.

The instructions available in data state differ in operation from those in control state in a significant way. The instructions in data state do not have OP codes such as those associated with instructions in control state. For this reason, the 3-bit mode register is set before entering data state. There are eight possible modes.

Once the display control enters data state; for instance in mode 0 (point mode), each pair of words taken from memory is treated as a point-mode instruction until the escape bit is set in one of the word pairs. The escape bit causes the display to return to control state. Control-state instructions are then executed until the system reenters data state in the execution of a control-state command code 1 or 3.

In data state, the cycles are called S1 and S2. The two-word modes are point mode, vector mode, and vector-continue mode. In S1 the first word is read from memory; in S2 the second word is read. When the instruction is executed, the operation reverts to S1. In the one-word modes, which are graphplot mode, increment mode, character mode, and short-vector mode, only S1 is used.

CHAPTER 4
OPERATION AND PROGRAMMING INFORMATION

This chapter describes system controls and indicators and furnishes information on the display system operating procedures.

4.1 SYSTEM CONTROLS AND INDICATORS

The system operating controls consist of the operator's console of the PDP-9 computer (fully described in DEC document F-95), the pushbuttons of the control box (Figure 4-1), and the light pen. Major register and status indicator lights are shown in Figure 4-2.

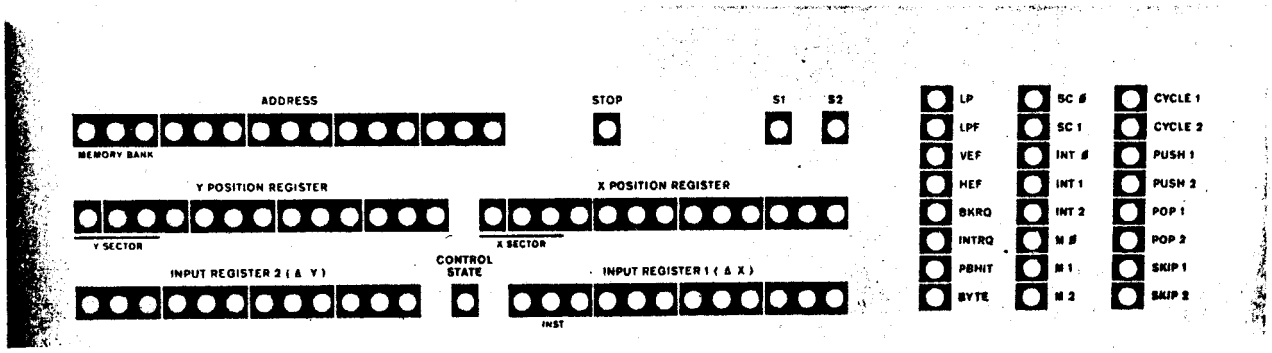


Figure 4-1 Control Box Panel

Table 4-1 lists the identification and function of each of the controls and indicators shown in these Figures 4-1 and 4-2.

The control panel illuminating type pushbuttons are arranged in two banks of six. Each bank can be reset by depressing the associated clear (CLR) button. Within a bank of six only one can be pressed because of mechanical interlocking, but single buttons from each bank can be pressed simultaneously. Complementing flip-flops are associated with the pushbuttons of the pushbutton logic. A pushbutton is lit when the flip-flop is in the 1 state.

Communication exists between these buttons and the operator, the display logic, and the PDP-9. The operator can read the status of the flip-flops by the switch lights, the display logic senses the status by using control-state skip instruction (Paragraph 4.5), and the PDP-9 can read the pushbutton states into the accumulator. The PDP-9 and display can also clear and set the pushbutton flip-flops.

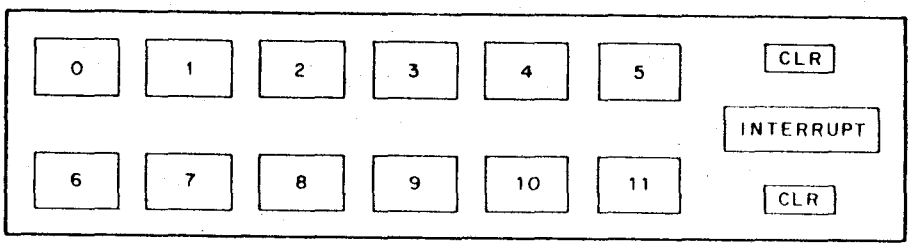


Figure 4-2 Type 339 Display, Indicator Panel

Table 4-1
Controls and Indicators

Switch	Function
	Control Box
0-11	Switches are associated with flip-flops PBF0-11, respectively. Pushing a button causes a pushbutton hit flag.
INTERRUPT	Provides a manual interrupt facility.
	Indicator Panel
Light	Function
MEMORY BANK	Three binary indicators that identify the 4096-word memory field being addressed
ADDRESS	Display 15 bits (including MEMORY BANK) of current memory address
STOP	Indicates external stop flag on
S1, S2	The two cycles used in data state, when information is presented to the CRT
Y SECTOR	State of 3 bits that provide sector addressing of 8 Y sectors*
Y POSITION REGISTER	State of 13 bits that provide direct address of 8192 Y points*
X SECTOR	State of 3 bits that provide sector addressing of X sectors*
X POSITION	State of 13 bits that provide direct address of 8192 X points*
INPUT REGISTER 2 (ΔY)	Indicates content of ΔY register
CONTROL STATE	Indicates display system in control state operation; change parameters, jump, skip, etc.

*See Section 4.3.1

Table 4-1 (cont.)
Controls and Indicators

Light	Function
	Indicator Panel (Cont.)
INST	Condition of 3 most significant bits of INPUT REGISTER 1 (ΔX) (identify current instruction).
INPUT REGISTER 1 (ΔX)	Indicates content of ΔX register
LP	Indicates light pen on (enabled)
LPF	Indicates light pen find flag
VEF	Indicates vertical edge flag (overflow or underflow in the Y register)
HEF	Indicates horizontal edge flag (overflow or underflow in the X register)
BKRQ	Indicates DMA break request is active
INTRQ	Indicates an interrupt request is active
PBHIT	Indicates pushbutton hit flag is on
BYTE	Indicates that the first byte of a word in the increment mode has been executed.
SC0	State of scale register bit 0*
SC1	State of scale register bit 1*
INT0	State of intensity bit 0
INT1	State of intensity bit 1 — Intensity bits provide selection of 8 intensity levels
INT2	State of intensity bit 2
M0	Mode bit 0
M1	Mode bit 1
M2	Mode bit 2
CYCLE 1	
CYCLE 2	
PUSH 1	Indicates which of eight control state cycles is about to be executed
PUSH 2	
POP 1	
POP 2	
SKIP 1	Indicates conditional skip 1 active
SKIP 2	Indicates conditional skip 2 active

*See Section 4.3.2.

4.2 LIGHT PEN OPERATION

By using the light pen, the operator of the CRT display can communicate immediately with the PDP-9 processor. The light pen is an input device that generates a signal (flag) that can be sensed and interpreted by the computer. When the light pen is positioned over a graphic and senses light, display operation ceases with the control logic retaining the X and Y coordinates at the point of light pen interruption. The light pen strike alerts the program via program interrupt or automatic priority interrupt, if the light pen flag enable bit has been previously set.

4.3 OPERATOR PROGRAMMING INFORMATION

The PDP-9 input-output transfer (IOT) instruction scheme provides computer communication with the I/O equipment, and the display is an I/O device to the computer. These IOT instructions, summarized in Paragraph 4.7, control initialization of the display, sense the state of the display, and restart the display after an interrupt.

Any portion of PDP-9 core memory can be reserved for display instructions which are arranged in core memory and constitute a display program. This arrangement can be either sequential or non-sequential (jumps). Instructions are transferred to the display system on demand by the display system via the PDP-9 DMA break facility.

Once it is started, the display control operates through the DMA break facility to fetch instructions (display program) to generate the raster. When the graphic is constructed, the last instruction in the sequence can be coded to stop operation. The subsequent program interrupt or automatic priority interrupt notifies the computer that the graphic is completed and the system is ready for further direction.

In normal computer programming, a program can call a subroutine to execute repetitive operations. Similarly, the display PUSH JUMP and POP instructions add subroutining capability for graphics. If a particular graphic, for example, a circle is to be drawn in many locations on the CRT, it is advantageous to use a single display instruction sequence to construct the circle each time. Therefore, whenever the circle is repeated, the same display sequence is called by the subroutine call display instructions. The display instruction repertory enables open and closed subroutine calls. Multilevel subroutines are likewise possible.

4.3.1 Display Parameters (Coordinate System)

The display screen is 9-3/8 in. square and has 1024 points in the X and Y directions (10 bits for X and 10 bits for Y), or about a million points. The X- and Y-position registers are 13 bits long, however, so the screen represents only 1/64 of the total addressable area (paper). The paper is broken up into 64 sectors corresponding to the upper 3 bits of X and Y, with sector 0 defined as the lower left sector.

Only information in sector 0 is intensified, so that translation is accomplished by moving the picture (or graphics) in relation to sector 0. The lower left corner is point (0,0), and the coordinates increase to the right and up to the upper right corner (1777_8, 1777_8).

An edge violation occurs when a line is drawn across the boundary of the paper. This is an indication that an overflow or underflow condition has just occurred in the X- or Y-position register. The horizontal edge flag indicates overflow or underflow in the X register; the vertical edge flag indicates overflow or underflow in the Y register. The overflow can be set to occur after the 10th, 11th, 12th, or 13th bit in X and Y. The effective paper size can therefore be changed under program control.

4.3.2 Scale

The scale setting determines the number of positions each succeeding spot is moved before becoming intensified. It affects both the size and appearance of lines or symbols drawn in the vector, vector-continue, short vector, increment, and character modes. At scale setting 11_2, each point can be clearly distinguished. At scale setting 00_2, line and symbols appear to be continuous. The point spacing is illustrated in Table 4-2.

Table 4-2
Intensity Scale

Scale	Point Spacing	Intensify
00_2	● ● ● ● ● ● ● ● ● ●	Every
01_2	● ○ ● ○ ● ○ ● ○ ● ○	2nd
10_2	● ○ ○ ○ ● ○ ○ ○ ● ○	4th
11_2	● ○ ○ ○ ○ ○ ○ ○ ● ○	8th

4.3.3 Intensity Level

Eight intensity levels are available on the display, ranging from 000_2, which is barely visible, to 111_2, which is very bright. Scale and intensity settings are interrelated. If characters are drawn (using the character generator) at the lowest scale setting, and too high an intensity level is used, the characters blur badly. On the other hand, if many characters are to be displayed simultaneously, or if the light pen is to be used, it is best to use as high an intensity level as practical. Intensity level 100_2 is normally bright enough for light pen operation.

4.3.4 State

The display logic is divided into two sections: data state and control state. Control-state commands are instructions to the display logic to change parameters, jump, skip, etc. Data-state

commands are instructions to move the beam via the X- and Y-position registers. When the display is initialized, the commands are accepted in control state until an enter-data-state command is given. The display returns to control state from data state by escaping. (An escape bit in the last data state command signals the display logic to return to control state.)

In control state, the first three bits (op code) designate the operation to be performed by the remaining nine bits. All eight op codes are used:

- 0 Parameter
- 1 Mode
- 2 Jump
- 3 POP
- 4 Conditional skip 1
- 5 Conditional skip 2
- 6 Miscellaneous (microprogrammed)
  - 0 Arithmetic compare 1
  - 1 Arithmetic compare 2
  - 2 Skip on flags
  - 3 Count (scale and intensity registers)
  - 4-7 Set slaves (optional)
- 7 AC line voltage synchronization

4.3.5 Mode

Data-state words are accepted in one of seven formats defined by the contents of the mode register. The data-state modes are as follows.

- 0 Point
- 1 Increment
- 2 Vector
- 3 Vector continue
- 4 Short vector
- 5 Character (optional), VC38
- 6 Graphplot
- 7 Character (optional), VA38

All these modes are entered from control state by the enter-data-state command. Each mode, however, has its own way of escaping back to control state. The mode register is cleared by the system power clear and by initialization of the display (IOT 701605).

4.3.6 Subroutining

The display has control-state commands that can modify the DAC. This flexibility enables unconditional display jumps (JUMP), jumps to subroutine (PUSH JUMP), and returns from subroutines (POP). The new address is specified by 15 bits which allows direct addressing of 32K of core memory. The JUMP and PUSH JUMP commands are specified by two consecutive 12-bit words. PUSH JUMP stores the return address, mode, intensity, scale, and light pen status on a pushdown pointer list which resides in the first 4K of the PDP-9 core memory. This information is automatically written into two locations in the format shown below.

Break Field			Light Pen Enable	Scale		Mode			Intensity		
6	7	8	9	10	11	12	13	14	15	16	17

First Word

Low Order 12-Bits of Memory Address											
6	7	8	9	10	11	12	13	14	15	16	17

Second Word

The information is placed in the address indicated by the pushdown pointer (PTR), which is a 12-bit register in the display logic. When a PUSH JUMP is executed, the PTR is incremented twice, adding a new entry to the PTR list. This allows multilevel and recursive subroutines in the display.

The POP command reads the last entry on the PTR list from core memory and gates it back to the appropriate registers. The display status can be inhibited, however, from being restored. The PTR is decremented twice during the POP instruction, making the pushdown list a last-in first-out stack.

4.3.7 Flags

Several special conditions arising in the display often require the attention of the PDP-9 processor. These conditions cause display flags that can interrupt the computer. The states of display flags are sensed by IOT skip instructions. The flags are as follows.

a. Internal stop

b. External stop

c. Edge

d. Light pen

e. Pushbutton hit

f. Manual interrupt

The flags can be separated into two groups. Flags (a) through (d) stop the display; flags (e) and (f) do not stop the display. Group 1 flags are cleared in one of three ways: initialization of a display sequence (IOT 1605); resuming from the point the display stopped (IOT 0724 or IOT 1604); and issuing a pulse to clear the flag if the display is no longer needed (IOT 1601). Power clear clears all display flags.

4.3.7.1 Internal Stop - Internal stop is set by a control-state command (1400). When the display stops, the DAC is already incremented and points to the location that follows the stop code. The PDP-9 skips, if the internal stop flag is on and IOT 0721 is executed. Execution of IOT 1604 (with the AC = 0) causes the display to resume from this point.

4.3.7.2 External Stop - The PDP-9 IOT 0704, with AC bits 6 and 10 at 0, causes the display to stop. When the display stops, the external stop flag is set, interrupting the computer if the interrupt system is on.

The time lapse between the IOT and the display stop is dependent upon the display command being executed when IOT 0704 was initiated. This entire command is executed before the display stops. If the command is a two-word instruction jump, vector, or point-mode command, both words are executed before the display stops. This allows simple resumption of the sequence, even if the display is used in the interim.

The external-stop flag causes the PDP-9 to skip when IOT 0701 is initiated (with AC bits 6 and 10 at 0). The display sequence can be resumed by initiating IOT 0724.

4.3.7.3 Edge - The edge is defined as the point at which the X- or Y-position registers overflow or underflow. The initial conditions of the display can be set so that all edges are ignored. In normal usage, the edge flag stops the display; when the edges are ignored, however, the display waits 35 μs and then resumes automatically. IOT 0724 restarts the display from the edge, if the display stops. IOT 0702 causes the PDP-9 to skip, if either the horizontal or vertical edge flag is on.

If an internal and external stop occur at the same time, only one of the stop flags is set according to the relative occurrence times.

When an external stop occurs, the fetch cycle for the next display word is performed, and therefore the DAC remains pointing to the next display word. Execution of IOT 0724 will cause the fetched word to be executed first.

4.3.7.4 Light Pen - The light pen flag stops the display when set by the light pen pulse. This occurs about 6 μs after the initial flash. The display logic, therefore, has time to execute several more points in the vector before it stops. The PDP-9 can skip on the light pen flag using IOT 0642. The vector or increment sequence can be resumed by using IOT 0724.

4.3.7.5 Pushbutton Hit - If any of the twelve pushbuttons are hit, the pushbutton hit flag is raised. This flag does not stop the display, but can cause a computer interrupt. The flag is cleared by IOT 0602, which reads back the status of the flag into the AC. IOT 0621 reads the state of the twelve pushbuttons into the accumulator. There is no skip IOT for the pushbutton hit flag.

4.3.7.6 Manual Interrupt - The manual interrupt flag is set by the interrupt button on the pushbutton box. This is an illuminating pushbutton, so that the button is lit whenever the flag is set. This flag does not stop the display. The flag can be cleared by IOT 0722, which also causes the program counter to skip, if the flag is set.

Four of the display flags must be gated onto the interrupt line by the initial condition IOT 0665. These flags are edge, light pen, pushbutton, and internal stop. The external stop and manual interrupt flags always cause an interrupt, if the interrupt system is on.

4.3.8 Timing

The display can take a DMA cycle at the maximum rate of one out of four memory cycles (once each 5.0 μs). This rate is maintained, if control state instructions are being executed.* All control state instructions except JUMP, PUSH JUMP, and POP are executed in one display cycle. The JUMP instruction requires two cycles because it is a two-word instruction. The PUSH JUMP is a four-cycle instruction: two cycles to get the instruction out, and two cycles to push the two status words away on the pushdown list. The POP instruction is a three-cycle instruction: one cycle to obtain the instruction and two to read the status words from the pushdown list.

In data state, the mode and the number of intensified points determine the execution time. In the incremental modes (increment, vector, short vector, and vector-continue), points are plotted at a rate of one every 1.1 μs, if intensified, or one every 300 ns, if nonintensified. Point and graphplot mode words are provided a 35-μs delay to allow the beam to settle, whether the point is intensified or not. If points are plotted in the same general area, as in a continuous curve, the delay for settling is only 8 μs. The small delay is given if, and only if, the previous point and the point being plotted have the same high-order 3 bits (of the low-order 10) in both the X and Y position. The time needed to fetch the information must then be added (one or two display cycles) to get the total execution time.

*See PDP-9 User Handbook (F-95) for details on the DMA break system.

The VC38 Character Generator (optional) plots at approximately 50 μs per character. This time is variable, depending on the number of intensified points in the character. Control characters are executed in two display cycles, except for carriage return which takes an additional 35 μs.

To estimate the time required to display a character, add up the time required for drawing the character, then add in 12 μs for a 6-bit character dispatch and 14 μs for a 7-bit character dispatch.

4.4 DIAGNOSTIC PROGRAMS

Diagnostic programs, designed to test specific functions within the PDP-9, are available and described in the PDP-9 Maintenance Manual. These include system input/output tests and MAINDEC routines to check the processor and core memory operation.

In addition, the diagnostic routines listed in Table 4-3 are designed to test specific functions within the 339 System. These, and the PDP-9 MAINDEC routines, are available as perforated paper tapes in readin mode (RIM) format. Each diagnostic routine tape is accompanied by a description of the program, procedures for using the program, and information on analyzing the program results to locate specific failures. Application of these routines are indicated at appropriate points in Chapter 4 of the PDP-9 Maintenance Manual, as they apply to preventive and corrective maintenance of the Type 339 System.

Table 4-3
Type 339 System MAINDEC Programs

MAINDEC Number	Title	Description
9A-D6JA-D	Push Jump Test	Test Push Jump instruction
9A-D6KA-D	POP Test	Tests Pop instruction
9A-D6OA-D	Lots of Little Pictures on the 9	Used for adjusting analog subsystem
9A-D6NA-D	VIS Buffer Test	Tests data state, primarily
9A-D6MA-D	Instruction Test	Tests control state, primarily
9A-D6QA-D	Character Generator Test	Tests character generator function (VC38)
9A-D6LA-D	339 Pushbutton Test	Tests Pushbutton Skip instruction

4.5 CONTROL STATE COMMAND FORMATS

Control state commands are instructions to the display logic to change a register, such as scale, DAC, mode, etc. Some of the commands change more than one register, so an enable bit is provided

for each function. If the enable bit is a 1, the associated register is reset to the appropriate value. If the enable bit is a 0, the associated register is unchanged independent of contents of the bit(s) following the enable bit. There is no restriction on the number of registers that can be changed with one instruction.

4.5.1 Parameter

Op Code: Parameter			Scale			Light Pen		Intensity			
6	7	8	9	10	11	12	13	14	15	16	17
0	0	0									

Parameter command is an instruction to change the scale, light pen, and intensity registers. When the light pen register is a 1, a light pen hit stops the display. If the light pen register is a 0, all light pen hits are ignored.

Bits	Interpretation
6-8	Op code: parameter
9	Enables scale change
10, 11	Determines one of four possible scale settings if bit 9 is a 1
12	Enables light pen change
13	Turns the light pen on when it is a 1, or off when it is a 0, provided bit 12 is a 1
14	Enables intensity change
15, 16, 17	Determines one of eight possible intensity settings if bit 14 is a 1

ASSOCIATED MNEMONICS AND VALUES

Mnemonic Symbol	Octal Code	Operation
LPOF	0040	Light pen off
LPON	0060	Light pen on
SC1	0400	Set scale to X1
SC2	0500	Set scale to X2

ASSOCIATED MNEMONICS AND VALUES (cont.)

Mnemonic Symbol	Octal Code	Operation
SC4	0600	Set scale to X4
SC8	0700	Set scale to X8
INT*	0010	Set the intensity

*INT enables only the change of intensity; a space then a number between 0 and 7 to indicate the desired intensity should follow. Any of the mnemonics of the same op code may be combined to form a compound command. A typical parameter command would be SC2 LPOF INT 4 which would have an octal value of 554.

4.5.2 Mode

Op Code: Mode			Stop Code	Clear Push-Button Flag	Mode				Clear Sector Bits	Clear Coord-inate Bits	Enter Data State
6	7	8	9	10	11	12	13	14	15	16	17
0	0	1									

The mode command has six separate functions. It can cause the display to stop and set the internal stop flag, clear pushbutton flag, set the mode register, clear sector bits, clear coordinate bits, or enter data state. Only the mode change has an enable bit to prevent its being changed.

Bits	Interpretation
6, 7, 8	Op code: mode
9	Stops the display and sets the internal stop flag when bit is a 1
10	Clears the pushbutton and manual interrupt flags when bit is a 1
11	Enables mode change
12, 13, 14	Determines one of eight possible mode settings if bit 11 is a 1
15	Clears only the high-order three bits in both the x- and y-position registers when bit is a 1
16	Clears only the low-order 10 bits in the x- and y-position registers when bit is a 1
17	When bit is 1, the next instruction is accepted as a data state word rather than control state. The display remains in data state until an escape is executed

ASSOCIATED MNEMONICS AND VALUES

Mnemonic Symbol	Octal Code	Operation
EDS	1001	Enter data state
CCB	1002	Clear coordinate bits
CSB	1004	Clear sector bits
POINT	1100	Set mode to 0
INCR	1110	Set mode to 1
VEC	1120	Set mode to 2
VECON	1130	Set mode to 3
SVEC	1140	Set mode to 4
CHAR	1150	Set mode to 5
GRAPH	1160	Set mode to 6
CLDF	1200	Clear flag
STOP	1400	Stop display

4.5.3 Jump

Op Code: Jump			Scale			Light Pen		Push	Break Field		
6	7	8	9	10	11	12	13	14	15	16	17
0	1	0									

First Word

Low Order			12 Bits of Address								
6	7	8	9	10	11	12	13	14	15	16	17

Second Word

The jump command is a two-word (24-bit) instruction, 15 bits of which specify the new address. The 15 bits used are the last 3 bits in the first word, which specifies the memory field, and the entire second word, which specifies the address in one of the 4K memory fields. If bit 14 is a 1, the command Causes two words to be entered on the end of the pushdown pointer (PTR) list. The jump command can also change the scale and light pen registers.

Bits	Interpretation
6, 7, 8	Op code: jump
9	Enables scale change
10, 11	Determines one of four possible scale settings if bit 9 is a 1
12	Enables light pen change
13	Turns the light pen on when it is a 1, or off when it is a 0, provided bit 12 is a 1
14	When bit is a 0, the command is a simple jump, the scale and light pen are changed, and the new 15-bit address is inserted in the DAC and the display continues from there. When bit is a 1, the command is a push jump. The old address and the status of the display are stored on the PTR list; then the new address and scale or light pen change is inserted.
15, 16, 17	Specifies the high-order 3 (of 15) address bits for the jump or push jump command
Second Word	
6, 7, 17	Specifies the low-order 12 (of 15) address bits for the jump or push jump command

ASSOCIATED MNEMONICS AND VALUES

Mnemonic Symbol	Octal Code	Operation
JUMP	2000	Jump to 15-bit address contained in last digit and the next word addressed
PJMP	2010	Jump to subroutine addressed the same as JUMP
LPOF	0040	Light pen off
LPON	0060	Light pen on
SC1	0400	Set scale to X1
SC2	0500	Set scale to X2
SC4	0600	Set scale to X4
SC8	0700	Set scale to X8

4.5.4 Pop

								Inhibit Restoring			
Op Code: Pop			Scale			Light Pen		Mode	Light Pen and Scale	Intensity	Enter Data State
6 0	7 1	8 1	9	10	11	12	13	14	15	16	17

The pop command is the last word in a subroutine file. It causes the display to bring out the old address and old status from the PTR list. The status can be blocked from being reinserted by raising bits 14, 15, and/or 16. The new light pen and scale settings in the pop will always be inserted after the status is restored. The first instruction after the push jump can be a data state instruction by entering data state during the pop.

Bits	Interpretation
6, 7, 8	Op code: pop
9	Enables scale change
10, 11	Determines one of four possible scale settings if bit 9 is a 1
12	Enables light pen change
13	Turns the light pen on when it is a 1, or off when it is a 0, provided bit 12 is a 1
14	The mode status from the PTR list will not be restored when bit is a 1
15	The light pen and scale status from the PTR list will not be restored when bit is a 1
16	The intensity status from the PTR list will not be restored when bit is a 1
17	The display will be in data state when the word at the address taken from PTR list is executed.

ASSOCIATED MNEMONICS AND VALUES

Mnemonic Symbol	Octal Code	Operation
POP	3000	Exit from subroutine to next address after PJMP
PEDS	3001	Pop and enter data state

ASSOCIATED MNEMONICS AND VALUES (cont.)

Mnemonic Symbol	Octal Code	Operation
PNI	3002	Pop and inhibit resotring intensity
PNLS	3004	Pop and inhibit restoring light pen and scale
PNM	3010	Pop and inhibit restoring mode
LPOF	0040	Light pen off
LPON	0060	Light pen on
SC1	0400	Set scale to X1
SC2	0500	Set scale to X2
SC4	0600	Set scale to X4
SC8	0700	Set scale to X8

4.5.5 Conditional Skip (Bank 1)

Op Code: Conditional Skip (Bank 1)			Sense of Test	Clear Bits After Test	Complement Bits After Test	Selected Pushbuttons 0-5					
						PB0	PB1	PB2	PB3	PB4	PB5
6 1	7 0	8 0	9	10	11	12	13	14	15	16	17

All display skip commands skip two display words. The display skips two instructions so that a JUMP or PJMP command (which are two words long) can be executed or not executed properly. The pushbuttons to be tested should have 1's in the proper bits of the skip command. Using the clear and complement facilities, the pushbuttons can be set in any desired configuration. The sense test bit determines whether the user is testing for 1's or 0's.

Bits	Interpretation
6, 7, 8	Op code: conditional skip (bank 1)
9	If bit is 0, the display skips two words if any of the indicated pushbuttons are 0. If bit is 1, the display skips two words if any of the indicated pushbuttons are 1.
10	Sets all the selected pushbuttons to the 0 state (light off) when it is a 1, independent of the outcome of the test.
11	Complements all the selected pushbuttons after the test when it is a 1, independent of the outcome of the test. Since the pushbuttons are cleared before they are complemented, they can be set to the 1 state by having both bits 10 and 11 at 1.
12-17	Selected pushbuttons of bank 1; e.g., bit 12 = pushbutton 0, bit 11 = pushbutton 5.

ASSOCIATED MNEMONICS AND VALUES

Mnemonic Symbol	Octal Code	Operation
SK1	4000	Skip if any of the selected buttons are 0
INV	0400	Invert sense of test (skip if any selected button is 1)
CLAT	0200	Clear buttons tested after test
COAT	0100	Complement buttons tested after test

4.5.6 Conditional Skip (Bank 2)

Op Code: Conditional Skip (Bank 2)			Sense of Test	Clear Bits After Test	Complements Bits After Test	Selected Pushbuttons 6-11					
						PB6	PB7	PB8	PB9	PB10	PB11
6 1	7 0	8 1	9	10	11	12	13	14	15	16	17

This command is identical to conditional skip (bank 1) except that it tests pushbuttons 6 through 11.

Bits	Interpretation
6, 7, 8	Op code: conditional skip (bank 2)
9	
10	Same as conditional skip (bank 2)
11	
12-17	Selected pushbuttons of bank 2; e.g., bit 12 = pushbutton 6, bit 17 = pushbutton 11.

ASSOCIATED MNEMONICS AND VALUES

Mnemonic Symbol	Octal Code	Operation
SK2	5000	Skip if any of the selected buttons are 0
INV	0400	Invert sense of test (skip if any of the selected buttons are 1)
CLAT	0200	Clear pushbuttons tested after test
COAT	0100	Complement pushbuttons tested after test.

4.5.7 Miscellaneous

4.5.7.1 Arithmetic Compare Pushbuttons (Bank 1)

Op Code Miscellaneous			Microprogrammed: Arithmetic Compare PB (0-5)			Pushbuttons (0-5)					
						PB6	PB7	PB8	PB9	PB10	PB11
6	7	8	9	10	11	12	13	14	15	16	17
1	1	0	0	0	0						

Bits 12-17 of this command are compared to the contents of pushbuttons 0-5 (bank 1). If all the bits and pushbuttons match, the test succeeds and the display follows a normal sequence. If the test fails, the display skips two words.

4.5.7.2 Arithmetic Compare Pushbuttons (Bank 2)

Op Code: Miscellaneous			Microprogrammed: Arithmetic Compare PB (6-11)			Pushbuttons (6-11)					
						PB6	PB7	PB8	PB9	PB10	PB11
6	7	8	9	10	11	12	13	14	15	16	17
1	1	0	0	0	1						

Same instruction as above, except bits 12-17 are compared to pushbuttons 6-11.

4.5.7.3 Skip on Flag

Op Code: Miscellaneous			Microprogrammed: SKIP ON FLAG			Skip Uncon-ditional	Skip if Not Sector 0	Skip on Pushbutton Hit Flag		SKIP ON	Clear
								Bank 1	Bank 2	LPSI	LPSI
6	7	8	9	10	11	12	13	14	15	16	17
1	1	0	0	1	0						

All the commands will skip two words. Sector 0 is defined as any point where the x- and y-position registers have all 0's in the high-order 3 bits (of 13). The pushbutton hit flag causes skips on the individual banks (1 or 2). Both flags are cleared by IOT 0602 or by the display command CLDF (1200_8).

The light pen sense indicator (LPSI) is a special light pen flag which is set whenever the light pen senses light. This action is independent of the status of the light pen enable flag. Bits 16 and 17 control testing and clearing of the LPSI. When both bits are 1, the sense of the skip is determined before the LPSI is cleared. The LPSI cannot be cleared or tested by the PDP-9.

Bits	Interpretation
9, 10, 11	Microprogrammed: skip on flag
12	Do not execute the next two display words if bit is 1.
13	Do not execute the next two words unless the high-order three bits of both the x- and y-position registers are 0; i.e., skip if the beam is not on the screen.
14	Skip if any pushbutton 0-5 has not been pushed.
15	Skip if any pushbutton 6-11 has not been pushed.

Bits	Interpretation
16	Skip if the light pen sense indicator is a 0.
17	Spare Clear light pen sense indicator flag.

4.5.7.4 Count

Op Code: Miscellaneous			Microprogrammed: Count			Count Scale		Count Intensity		Blink On	Blink Off
6	7	8	9	10	11	12	13	14	15	16	17
1	1	0	0	1	1						

The scale and intensity registers are also up-down counters. They cannot overflow, however; the scale register stays at 11_2 no matter how many count scale up commands are given. The blink facility allows the picture or any section of it to flash on and off at 1 c/s (1/2 sec with the intensity on and 1/2 sec with the intensity off).

Bits	Interpretation
6, 7, 8	Op code: miscellaneous
9, 10, 11	Microprogrammed: count
12	Enables count scale logic
13	0: count scale up (unless at 11_2) 1: count scale down (unless at 00_2)
14	Enables count intensity logic
15	0: count intensity up (unless at 111_2) 1: count intensity down (unless at 000_2)
16	Turn blink on, all intensified points will be gated through the blink logic.
17	Turn blink off

4.5.7.5 Slave Logic (Optional)

Op Code: Miscellaneous			Micro Slaves	Group Number		Unit 0			Unit 1		
6	7	8	9	10	11	12	13	14	15	16	17
1	1	0	1								

The Slave Logic allows the display to control up to eight CRTs (seven slaves and one master). The slave logic blanks or unblanks the intensity and light pen at each CRT for the display file being executed until the slave status is changed. IOT 0622 and IOT 1642 can read back the status of the eight slaves into the PDP-9 (see Paragraphs 4.7.1.8 and 4.7.1.9).

Bits	Interpretation
6, 7, 8	Op code: miscellaneous
9	Specifies slave logic when it is a 1
10, 11	Choose one of four slave groups, with two units each, to be modified.
12	Enables change of unit 0 of slave group specified in bits 10,11
13	Turns on light pen of unit 0 if bit is a 1; turns it off if bit is a 0
14	Turns on the intensity of unit 0 if bit is a 1; turns it off if bit is a 0
15	Enables change of unit 1 of slave group specified in bits 10, 11
16	Turns on light pen of unit 1 if bit is a 1; turns it off if bit is a 0
17	Turns on the intensity of unit 1 if bit is a 1; turns it off if bit is a 0

ASSOCIATED MNEMONICS AND VALUES

Mnemonic Symbol	Octal Code	Operation
SK3	6000	Arithmetically compares pushbuttons (0-5) with last two digits of instruction; skip if not equal.
SK4	6100	Same as SK3 but for buttons 6 through 11
SKIP	6240	Unconditional skip (two locations)
SNSZ	6220	Skip if sector 0 flag is not up
SPB1	6210	Skip if pushbutton (0-5) flag is down
SPB2	6204	Skip if pushbutton (6-11) flag is down
SLPSI	6202	Skip if LPSI is off
CLPSI	6201	Clear LPSI
SCUP	6340	Count scale up

ASSOCIATED MNEMONICS AND VALUES (cont.)

Mnemonic Symbol	Octal Code	Operation
SCDN	6360	Count scale down
INTUP	6310	Count intensity up
INTDN	6314	Count intensity down
BKON	6302	Blink on
BKOF	6301	Blink off
SG0	6400	Set slave group 0
SG1	6500	Set slave group 1
SG2	6600	Set slave group 2
SG3	6700	Set slave group 3
SU0	0040	Turn light pen and intensity off on unit 0
LP0	0060	Unit 0 light pen on
IT0	0050	Unit 0 intensity on
SU1	0004	Turn light pen and intensity off on unit 1
LP1	0006	Unit 1 light pen on
IT1	0005	Unit 1 intensity on

4.5.7.6 AC Synchronization Control

Op Codes AC Sync			Spares							Skip on Idle Flag	Clear Idle Flag
6	7	8	9	10	11	12	13	14	15	16	17

The AC synchronization control command may be used to eliminate the often observed "swimming" of information on the screen due to local electromagnetic fields. The output of the CRT is synchronized with the input line voltage.

To use this synchronizing feature, the following code may be inserted at any point in the display files.

EXAMPLE: Insert at location 1500

```
1500:  7001     /CLEAR IDLE FLAG
       7002     /SKIP ON IDLE FLAG
       2000     /JUMP TO
       1501     /1501
```

Bits	Interpretation
6-8	Op Code: AC Sync
9-15	Spare
16	Skip on Idle Flag
17	Clear Idle Flag

4.6 DATA STATE COMMAND FORMATS

All data state commands change the x- and y-position registers which are in turn connected through D-A converters to the CRT deflection system. The mode register determines the data state mode to be used by the display. Only the mode command in the control state chan change this mode. Each of the eight possible modes has an escape mechanism to return to control state. Since most of the modes are different, each is described below.

Point, vector, and vector-continue modes are two-word commands; a single command is specified by two consecutive locations in the display list. Both words must be brought out before execution, and therefore there are two input buffer registers. The register ΔX, which is used for all commands, receives its information directly from the data lines. If the command is two words long, the first input word is transferred to the ΔY register while the second input word is brought in to ΔX from memory. The only exception to this is data state increment mode words. In this case, a single word command is executed from the ΔY register. The ΔX register is used for double buffering virtually eliminating the wait for input words. Short vector mode uses the ΔY register in order to appear as a normal vector. In other words, the ΔY portion of the command is transferred to the ΔY register.

4.6.1 Point Mode (Two Words)

Point		(000)									
Intensify	Inhibit	Y Position									
6	7	8	9	10	11	12	13	14	15	16	17

First Word (ΔY)

Point		(000)									
Escape	Inhibit	X Position									
6	7	8	9	10	11	12	13	14	15	16	17

Second Word (ΔX)

The basic action is to jam bits 8 through 17 of the first word (from ΔY) into the low-order 10 bits of the y-position register, and the same bits in the second word into the x-position register. The high-order three bits in x and y remain unchanged. If bit 7 in either word is up, the contents of the associated position register are not changed during that command. This is useful if the user does not know the present beam position and wishes to change either x or y and leave the other at the same value. If bit 6 in the first y point word is a 1, the point specified is intensified when the beam reaches the proper position. If bit 6 in the second word (x point) is a 1, it indicates an escape and the next word is interpreted as a control state command. If the bit is a 0, the next word is interpreted as the first word of another point mode command. The scale setting has no effect in point mode.

Word	Bit	Interpretation
1	6	If bit is a 1, intensify given point
	7	Inhibit changing y-position register
	8-17	New y coordinate (low-order 10 bits)
2	6	Escape to control state
	7	Inhibit changing x-position register
	8-17	New x coordinate (low-order 10 bits).

4.6.2 Increment Mode

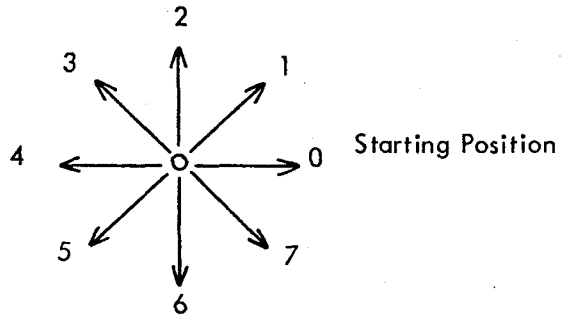
Increment 001											
Intensify	No. of Moves		Direction (0-7)			Intensify	No. of Moves		Direction (0-7)		
6	7	8	9	10	11	12	13	14	15	16	17

Increment mode is a mechanism for moving the beam a short distance in an efficient manner. The beam is moved from its previous position to a new position according to two 6-bit increment bytes. Each byte is handled separately and executed independently of the other. Both bytes (first, 6-11, second, 12-17) are identical; therefore only the first will be discussed.

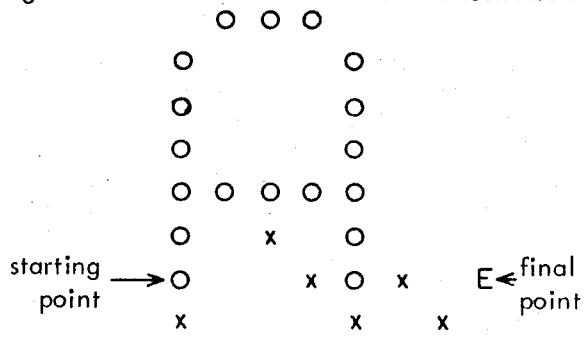
The byte is broken into three sections: first, to indicate whether the byte move is to be intensified (bit 6 (12)); second, to give the number of moves to be made (bits 7, 8, (13, 14)); and third, to specify the direction in which the move is to be made (bits 9, 10, 11, (15, 16, 17)). The beam is only intensified at discrete points according to the scale setting (see Paragraph 4.3.2), it is not intensified during the motion. The increment can consist of one, two, or three moves per byte, with each move being one, two, four, or eight points apart on the raster depending on the scale. The two bits that control the number of moves are programmed as follows.

Bits 7, 8	Interpretation
00	Move the beam once in the indicated direction and escape
01	Move the beam once; do not escape
10	Move beam twice; do not escape
11	Move beam three times; do not escape

The three bits for direction indicate one of eight 45 degree directions.



The letter "A" is programmed in subroutine form as an illustration of the use of increment mode.



The "o" indicates an intensified point, the "x" a nonintensified point, and "E" the point at which the escape is given.

```
ALPHAA,   INCR   EDS    /OCTAL (1111)
          1672          /BYTE 1 - ↑, 1 M, NONINTEN. BYTE 2 - ↓, 3 M, INTEN.
          7251          /BYTE 1 - ↑, 3 M, INTEN. BYTE 2 - ↗, 1 M, INTEN.
          6057          /BYTE 1 - →, 2 M, INTEN. BYTE 2 - ↘, 1 M, INTEN.
          7674          /BYTE 1 - ↓, 3 M, INTEN. BYTE 2 - ←, 3 M, INTEN.
          3762          /BYTE 1 - ↘, 3 M, NONINTEN. BYTE 2 - ↑, 2 M, INTEN.
          2701          /BYTE 1 - ↘, 2 M, NONINTEN. BYTE 2 - ↗, 1 M,
                        /NONINTEN. AND ESCAPE
          POP           /OCTAL (3000)
```

Bits	Interpretation
6	If bit is a 1, intensify the first byte.
7, 8	Number of moves in the byte (00_2 => Move once and escape)
9, 10, 11	Direction in which moves are to be made
12	If bit is a 1, intensify the second byte.
13, 14	Same structure as byte 1 bits 7 and 8
15, 16, 17	Same structure as byte 1 bits 9, 10, 11

4.6.3 Vector Mode (Two Words)

Vector (010)											
Intensify	+ −	10-Bit ΔY									
6	7	8	9	10	11	12	13	14	15	16	17

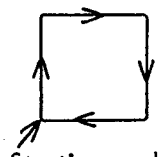
First Word (ΔY)

Vector		(010)									
Escape	+ −	10-Bit ΔX									
6	7	8	9	10	11	12	13	14	15	16	17

Second Word (ΔX)

Vector mode is used to draw long straight lines. The beam is moved from its present location in the direction and distance specified by the Δy and Δx. The deltas tell the beam how many moves to make in x and y before stopping. The number of raster points between each move is again dependent upon the contents of the scale register. At a scale of 1, the 10-bit vector can take the beam from one end of the screen to the other. At a scale of 8, the beam can go to any point on the 13-bit "page". Bit 7 in both words indicates the sign (direction) of the vector. A + is indicated by a 0 and is up for y and to the right for x. Bit 6 in the first word indicates whether the vector is to be intensified. Bit 6 in the second word is the escape to control state which indicates the end of a vector string.

The following display subroutine program places on the screen a 1-in. square. Since the box is drawn with vectors, it can be put anywhere on the screen (relocatable).




```
IBOX,   SC2 INT 5       /CONTROL STATE OCTAL (515)
        VEC EDS         /CONTROL STATE OCTAL (1121)
        4067            /Δy = +55.  INTENSIFY
        0000            /Δx =   0.
        4000            /Δy =   0.  INTENSIFY
        0067            /Δx = +55.
        6067            /Δy = -55.  INTENSIFY
        0000            /Δx =   0.
        4000            /Δy =   0.  INTENSIFY
        6067            /Δx = -55.  ESCAPE
        POP             /CONTROL STATE OCTAL (3000)
```

Word	Bits	Interpretation
1	6	If bit is a 1, intensify the vector.
	7	If bit is a 0, the sign of Δy given in bits 8-17 is positive; if a 1, it is negative.
	8-17	The 10-bit Δy
2	6	If bit is a 1, the next word is interpreted in control state.
	7	If bit is a 0, the sign of Δx given in bits 8-17 is positive, if a 1, it is negative.
	8-17	The 10-bit Δx.

4.6.4 Vector Continue Mode (Two Words)

Vector Continue (011)											
Intensify	+ −	10-Bit ΔY									
6	7	8	9	10	11	12	13	14	15	16	17
Escape		10-Bit ΔX									
6	7	8	9	10	11	12	13	14	15	16	17

Vector-Continue mode has the same format and action as vector mode, except the vector does not stop until it violates the edge. This will not cause an edge flag to be set.

4.6.5 Short Vector

Short Vector (100)											
Intensify	+ −	ΔY				Escape	+ −	ΔX			
6	7	8	9	10	11	12	13	14	15	16	17

Short vector mode is basically the same as vector mode except that it is only one word long. To fit it into one word, the maximum number of increments has been reduced from 1024 to 16 in x and y directions. Bits 6 and 7 of a short vector word correspond to bits 6 and 7 of the first word of a vector command. Bits 8, 9, 10, and 11 correspond to 14, 15, 16, and 17 of the first word; bits 12 and 13 to bits 6 and 7 of the second word; and bits 14, 15, 16, and 17 to bits 14, 15, 16, and 17 of the second word. In execution of a short vector mode command, the left half of the input word is transferred to ΔY and bits are rearranged to be in the same format as a vector mode command.

Bits	Interpretation
6	If bit is a 1, intensify the vector.
7	If bit is a 0, the sign of Δy in bits 8, 9, 10, and 11 is positive; if a 1, it is negative.
8,9,10,11	The 4-bit Δy.
12	If bit is a 1, the next word is interpreted in control state.
13	If bit is a 0, the sign of Δx given in bits 14, 15, 16, and 17 is positive; if a 1, it is negative.
14,15,16,17	The 4-bit Δx.

4.6.6 Character Mode (Optional)*

Character (101)*											
Character 1						Character 2					
6	7	8	9	10	11	12	13	14	15	16	17

Six-bit format

Ignored					Character						
6	7	8	9	10	11	12	13	14	15	16	17

Seven-bit format

The character generator can be run in two different formats: 6-bit format, packed two to a word but directly referencing only 64 characters; or 7-bit format, only one character per word but referencing 128 different characters. The character generator is simply an efficient dispatch system for instructions stored in core memory. The characters, therefore, are programmable as well as the dispatch table that calls them. The details of programming the character generator are given in Appendix A.

Special characters available in the character generator include set and count intensity and scale, set light pen, change case, change character set, change code size (6-bit versus 7-bit), carriage return (clear x register), and escape to control state.

*Hardware character mode (111) is identical in operation to the 6-bit format described here.

4.6.7 Graphplot Mode

Graphplot (110)											
Escape	Set Y Set X	X or Y Coordinate									
6	7	8	9	10	11	12	13	14	15	16	17

Graphplot mode is a concise way of describing and displaying tabular data. The execution of a data command is as follows. First, the x or y coordinate is incremented once; then the other coordinate is set by bits 8-17 of the graphplot mode command. Bit 7 of the word specifies whether x is to be incremented and y plotted (bit 7-0), or y incremented and x plotted (bit 7-1). If bit 6 is a 1, the display escapes to control state.

The incremented axis moves one, two, four, or eight points depending on the scale setting. Since one axis is always incremented, the graph is easily translated in this direction by changing the starting location.

Bits	Interpretation
6	If bit is a 1, escape to control state.
7	If bit is a 0, increment x coordinate and set the y coordinate with bits 8-17; if bit is a 1, increment y and set x.
8-17	Ten bits of coordinate information

4.7 DISPLAY ORIENTED COMPUTER INSTRUCTIONS

The PDP-9 has a family of instructions* which it uses to communicate with I/O equipment. A group of these instructions is assigned to the display (IOTs 05, 06, 07). Given below are the display IOTs, their mnemonics, and their functions. They are divided into three classes: the first requests information from the display; the second sends information to the display; and the third causes computer skips on display flags. Information transfers go through the PDP-9 accumulator; if the user expects information, he should clear the AC beforehand, and if sending information, he should have the data in the AC before giving the IOT.

*See PDP-9 User Handbook for details.

4.7.1 Group 1. From the Display

4.7.1.1 RPDP 700501 Read Pushdown Pointer - Performs a 1s (inclusive OR) transfer from the pushdown pointer (12 bits) to the AC. The PTR should be pointing to the location in which status information will go on the next push jump (if it comes before a pop). Reading the PTR, subtracting the set value, and dividing by two gives the level of the subroutine.

4.7.1.2 RXP 700502 Read x-Position Register - Performs a 1s transfer from the x-position register to the AC. Only the low-order 12 (of 13) bits are transferred; the high-order bit must be obtained from the RS2 instruction.

4.7.1.3 RYP 701602 Read y-Position Register - Same as RXP, except the y-position register is transferred.

4.7.1.4 RDAC 700601 Read Display Address Counter - The contents of the display address counter are transferred from the display to the AC. The DAC will be set at the next command to be executed by the display.

4.7.1.5 RS1 700602 Read Status 1 - Status 1 consists of the state of all display flags and the contents of the break field register. If the flag is up the associated bit is a 1. After the IOT is given the push-button flag will be cleared. The IOT reads back the old state of the flag into AC bit 13.

RS1

L.P. Hit Flag	Vertical Edge Flag	Hori-zontal Edge Flag	Internal Stop Flag	Sector Zero Flag	Control State Flag	Manual Inter-rupt Flag	P.B. Hit Flag	Display Inter-rupt Flag	Break Field		
6	7	8	9	10	11	12	13	14	15	16	17

Bits	Interpretation
6	Light pen hit flag
7	Vertical edge flag. The y-position register has overflowed.
8	Horizontal edge flag. The x-position register has overflowed.
9	Internal stop flag
10	Sector 0 flag. If bit is a 1, the display is in sector 0.
11	Control state flag. If bit is a 1, the display is in control state, if it is a 0 the display is in data state.
12	Manual interrupt flag
13	Pushbutton hit flag
14	Display interrupt flag. If the interrupt system is turned on and bit is a 1, the computer will interrupt. It is set by one of the six display flags being on and gated onto the interrupt line.
15,16,17	Contents of break field register. These 3 bits and the 12 bits from the RDAC instruction give the full 15-bit memory address.

4.7.1.6 RS2 701622 Read Status 2 - Status 2 consists of the contents of some of the major registers in the display; e.g., light pen, scale, mode, and intensity. It also contains byte information and the high-order bit of the x- and y-position registers. The byte flip-flop indicates whether the left half or right half byte in increment mode was being executed when the display stopped. It does not tell whether the right- or left-hand character is being executed; this information is obtained from the RCG (IOT 1662) instruction. The low-order 12 bits of the 13-bit x- and y-position register are obtained by giving RXP or RYP.

RS2

Byte	L.P. Enable	Y Position Bit 0	X Position Bit 0	Scale		Mode			Intensity		
6	7	8	9	10	11	12	13	14	15	16	17

6	Byte flip-flop. If bit is a 0, the left-hand increment is being executed; if bit is a 1, the right-hand byte is being executed.
7	Light pen enable. If bit is a 1, the light pen is enabled.
8	High-order y-position register bit.
9	High-order x-position register bit.
10,11	Scale
12,13,14	Mode
15,16,17	Intensity

4.7.1.7 RPB 700621 Read Pushbuttons - The contents of the 12 pushbuttons (0-11) are transferred into AC bits 6-17.

4.7.1.8 RSG1 700622 Read Slave Group 1 - On this instruction, the light pen enable, light pen hit, and intensity status for slaves 0, 1, 2, and 3 are read into the AC. The control state command "set slaves" sets the light pen and intensity status. If the slave option is not present, the IOT reads back 0's into the accumulator.

Slave 0			Slave 1			Slave 2			Slave 3		
Light Pen	Intensity	Light Pen Hit									
6	7	8	9	10	11	12	13	14	15	16	17

AC Format

Bits	Interpretation
6	Light pen enable, slave 0
7	Intensity status of slave 0
8	Light pen hit, status slave 0
9,10,11	Same format as above for slave 1
12,13,14	Same format as above for slave 2
15,16,17	Same format as above for slave 3

4.7.1.9 RSG2 701642 Read Slave Group 2 - RSG2 has the same format as RSG1, except it reads the status of slaves 4, 5, 6, and 7.

4.7.1.10 RCG 701662 Read Character Generator - RCG reads in the five character generator parameters: character generator active (CHACT), character byte (CB), case, code size (CHSZ), and starting address register (SAR). The CHACT bit indicates whether the character generator is in use; i.e., the display is in character mode and data state. The CB shows whether the left or right character (6-bit format) is being executed. The case bit is used (6-bit format) as a seventh bit to allow referencing either the lower or upper set of 64 characters. The CHSZ indicates whether the 6-bit or 7-bit character format is to be used. The SAR is a 6-bit register that indicates the starting address of the character dispatch table (Appendix A).

Char-acter	CB	Spare	Case	CHSZ	Spare	SAR					
6	7	8	9	10	11	12	13	14	15	16	17

Bits	Interpretation
6	If bit is a 1, the character generator is active
7	If bit is a 0, left character is being executed. If bit is a 1, right character is being executed.
8	Spare
9	If bit is a 1, upper case is in use, characters 65-128
10	If bit is a 0, the character generator is using 6-bit format; if bit is a 1, the CG is using 7-bit format.
11	Spare
12-17	Contents of the 6-bit SAR

4.7.2 Group 2. To the Display

4.7.2.1 SPTR 700645 Set the Pushdown Pointer - The contents of the AC are transferred into the PTR register. Since the PTR is a 12-bit register, the PTR list must reside in the first 4K of memory.

4.7.2.2 SIC 700665 Set Initial Conditions - SIC sets up a number of status registers in the display. The instruction enables four display flags onto the interrupt line, sets the page size to 10, 11, 12, or 13 bits in x and y and light pen conditions. One of three options are available in the event the display is resumed after a light pen hit. The light pen can be left on, it can be turned off completely, or it can be turned off until the completion of the present command, then automatically turned back on at the next data request. A register tells the display to ignore all edge flags; therefore when the position register overflows, the edge flag is inhibited and the display continues in a normal fashion. Another register overrides the intensification bit in data state, causing all beam movements to be intensified. This feature is used principally for diagnostic purposes.

SIC

Edge Interrupt	L.P. Interrupt	L.P. Resume Options		Y Dimension		X Dimension		Intensify All Points	Inhibit Edge Flags	P.B. Interrupt	Internal Stop Interrupt
6	7	8	9	10	11	12	13	14	15	16	17

Bits	Interpretation
6	Enable edge flag interrupt
7	Enable light pen flag interrupt
8	If bit is a 0, do not disable light pen after the resume; if bit is a 1, bit 9 indicates when to reenable the light pen
9	If bit is a 0, reenable light pen on the first data request after the display is resumed. If bit is a 1, the light pen hit is equivalent to a LPOF command.
10,11	Set y dimension 00: 9.375 in. (10 bits) 01: 18.75 in. (11 bits) 10: 37.5 in. (12 bits) 11: 75.0 in. (13 bits)
12,13	Set x dimension, same as y
14	Intensify all points
15	Inhibit edge flags
16	Enable interrupt on pushbutton hit
17	Enable interrupt on internal stop flag

4.7.2.3 LBF 700705 Load Break Field - This instruction has two functions. First, it loads the break field register when initializing the display; second, it sets the pushbuttons. Both functions have enable bits so that one may be executed without the other. If neither enable bit is up, the IOT pulses have other meanings (STPD-700704 and SPES-700701).

Break Field			Pushbuttons								
6	7	8	9	10	11	12	13	14	15	16	17

Bits	Interpretation
6	Enable change of break field
7,8,9	New break field
10	Enable change of pushbuttons
11	If bit is a 0, set pushbuttons 0-5 according to AC bits 12-17; if bit is a 1, set pushbuttons 6-11 according to AC bits 12-17.
12-17	New pushbutton states.

4.7.2.4 SCG 700743 Set Character Generator - SCG sets the SAR, Case and CHSZ.

Spare			Case	CHSZ	Spare	SAR					
6	7	8	9	10	11	12	13	14	15	16	17

Bit(s)	Interpretation
6,7,8	Spare
9	Set case 0-lower 64 1-upper 64
10	Set code size 0-6 bit character format 1-7 bit character format
11	Spare
12-17	Starting address register

4.7.2.5 INIT 701605 Initialize the Display - The display flags are cleared, the AC is transferred to the low-order 12 bits of the DAC, and the display is initialized by raising the break request flag. The display will run uninterrupted until a flag is raised.

INIT must not be executed when the display is running since it ignores the timing and causes random errors. If an external stop is used to stop the display before executing INIT, the display stopping time is dependent on execution of the display command, and INIT should not be executed until the external stop flag goes on.

```
INITIAL   LAC XPDP    /LOAD AC WITH CONTENTS OF XPDP
          SPDP        /IOT TO TRANSFER AC TO PDP
          LAC XSIC    /LOAD AC WITH CONTENTS OF XSIC
          SIC         /TRANSFER AC TO INITIAL CONDITION REGISTER
          LAC XLBF    /LOAD AC WITH CONTENTS OF XLBF
          LBF         /TRANSFER AC TO BF
          LAC XCG     /LOAD AC WITH CONTENTS OF XCG
          SCG         /IOT TO TRANSFER AC TO CG
          LAC XIN     /LOAD AC WITH CONTENTS OF XIN
          INIT        /IOT TO TRANSFER AC TO DAC AND INITIALIZE DISPLAY
          CLA         /CLEAR AC
          ION         /TURN INTERRUPT ON
          JMP.        /DISPLAY IS NOW RUNNING
XPDP      7000        /STARTING ADDRESS OF PUSHDOWN LIST
XSIC      2367        /ENABLE LIGHT PEN, PUSHBUTTON, AND INTERNAL STOP
                      /FLAGS; SET PAPER SIZE TO 75 IN. BY 75 IN. LEAVE LIGHT
                      /PEN ON AFTER LIGHT PEN HIT, AND ENABLE ALL EDGE
                      /FLAGS.
XLBF      4000        /THE DISPLAY PROGRAM STARTS IN MEMORY CORE ZERO.
                      /NOTE THE ENABLE BIT MUST BE A 1 TO CHANGE THE
                      /BREAK FIELD REGISTER.
XCG       0016        /SET CODE SIZE TO 6-BIT FORMAT, START IN THE LOWER
                      /CASE, AND THE CG DISPATCH TABLE STARTS IN LOCATION
                      /16000 (MEMORY BANK 1 LOCATION 6000).
XIN       DISSTT      /SYMBOLIC ADDRESS OF THE FIRST LOCATION IN THE DIS-
                      /PLAY FILE.
```

4.7.2.6 RES1 700724 Resume After Light Pen Hit, Edge, or External Stop Flag - This IOT tells the display to resume the sequence of instructions from the point at which it stopped. In the case of a light pen hit or edge flag, the display completes the vector it stopped on before continuing to the next. One of the above flags must be up when RES1 is given; otherwise, the instruction has no effect. RES1 clears the flag before the display is reinitialized. The contents of the AC have no effect during this instruction.

In the case of the external stop flag, the already fetched display word will be executed.

4.7.2.7 CFD 701601 Clear Display Flags - CFD clears the four flags that stop the display. This command is given when the display is not to be used any longer, but has been used in this program. The power clear pulse (START key) also clears all display flags. All display flags can be cleared by giving three IOTs: CFD-701601 (internal and external stop, light pen hit, and edge); RS1-700602 (pushbutton); and SPMI-700722 (manual interrupt). The DAC and Mode registers are cleared and the display is put in control state.

4.7.2.8 STPD 700704 Stop Display (External) - STPD stops the display and sets the external stop flag (see Paragraph 4.3.7) when the display has stopped. This is one of the microprogrammed IOTs and requires a 0 in bits 6 and 10 of the AC when the IOT is given.

4.7.3 Group 3. IOT Skip on Display Flags

4.7.3.1 SPLP 700642 Skip on Light Pen Hit Flag - Pertains only to the master scope's light pen. If the flag is up, the computer skips one instruction (i.e., two words).

4.7.3.2 SPSP 700662 Skip on Slave Light Pen Hit Flag - If any of the seven slave light pen flags are up, the computer skips. The particular display can be found by giving the RSG1 and RSG2 IOTs and interrogating the AC.

4.7.3.3 SPES 700701 Skip on External Stop Flag - This is a microprogrammed instruction and requires a 0 in bits 6 and 10 of the AC when the instruction is given. The next instruction is skipped if the external stop flag is on.

4.7.3.4 SPEF 700702 Skip on Edge Flag - SPEF causes a computer skip if either the horizontal or vertical edge has been violated. The edge violated can be found by giving the RS1 IOT. If the display runs off the corner of the page, both the horizontal and vertical edge flags will be up.

4.7.3.5 SPSF 700721 Skip on Any Display Flag - The computer skips if any display flag is on. Status Word 1 may be interrogated to determine which flag caused the skip.

4.7.3.6 SPMI 700722 Skip on Manual Interrupt - SPMI causes the computer to skip if the manual interrupt flag is on. It also clears the flag and the light in the pushbutton if it is up.

APPENDIX A
VC38 CHARACTER GENERATOR

The VC38 is a dispatch type generator, with both the dispatch table and the execution routines stored in core memory. The 6- or 7-bit character is used to index a special 15-bit register (CHAC) which contains the starting address of the dispatch table. The word from the referenced location is then used to index the CHAC to get to the location of the beginning of the variable length execution routine. At the end of the routine, an escape code is given which directs the CG (character generator) to accept the next character and restart the process. There are also special dispatch words (control characters) which do not cause a dispatch but rather are direct commands to the logic.

The beginning of the dispatch table is specified by the SAR (starting address register) which is 6-bits long. The SAR is gated to the upper six bits of the CHAC which in turn is gated onto the memory address (MA) bus. As an example, if the SAR contains 16_8, the dispatch table begins at location 6000_8 in core memory 1. The SAR is set and read by the PDP-9 via IOTs (SCG and RCG, respectively).

The characters are interpreted in 6- or 7-bit format depending on the contents of the 1-bit code size register (CHSZ). If the register is a 1, the low-order seven bits of the data word are gated into the low-order seven bits of the CHAC, and the SAR is gated into the CHAC to produce the dispatch table address. Thus, if the SAR is 04_8 and the character is 116_8, the word in location 4116_8 contains the dispatch address.

In the 6-bit format, an identical process takes place except that the leftmost six bits are first gated onto the CHAC and the right six bits are put in a character save (CS) register. The CS register is gated onto the low-order six bits of the CHAC when the first character is complete. The CB register is also set to a one, indicating execution of the left character.

Along with the six character bits, the CASE bit is gated into bit 11, allowing reference to 128 characters by a 6-bit character code.

CHAC (Six Bit Code Format)														
SAR						Set to Zero		Case	6 Bit Character Code					
3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

The dispatch word obtained from the location specified by the CHAC is interpreted in the same way whether the six or seven bit format was used.

In the dispatch word, bit position 6 indicates whether the dispatch table word is a control word (bit 6=1) or a dispatch word (bit 6=0). If it is a dispatch word, the character can be drawn in either increment or short vector mode. Bit 7 in the dispatch word indicates the mode. If the bit is 0, the data is accepted in increment mode; if it is 1, the data is accepted in short vector mode. The low-order 10 bits are used as the dispatch address and are gated onto the low-order 10 bits of the CHAC.

Dispatch Word											
	Mode	Address									
6 0	7	8	9	10	11	12	13	14	15	16	17

CHAC During Dispatch														
SAR					Over-lap	Dispatch Address								
3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Both the SAR and the dispatch address reference bit 8 in the CHAC. The bit is the inclusive OR of these two registers. In other words, if the SAR is odd (i.e., bit 8 is a 1), the dispatch address can only reference 512_{10} locations, whereas, if the SAR is even, the table can reference 1024_{10} locations.

A.1 CONTROL CHARACTERS

If the dispatch table word has bit 6=1, a dispatch does not take place, but rather the word is accepted in one of three spacial formats indicated by bits 7 and 8. After execution of the control character, the next character is immediately fetched.

A.1.1 Parameter Control

Parameter control format is specified by 00_2 in bits 7 and 8 of the dispatch table word. Bits 9-17 are then interpreted in the same format as the parameter mode word of control state.

Dispatch Table Word (Parameter Control)												
			Scale			Light Pen		Intensity				
6 1	7 0	8 0	9	10	11	12	13	14	15	16	17	

Bits	Interpretation
6	=1 Control character
7,8	$=00_2$ Parameter control
9	Enables scale change
10,11	Determine one of four possible scale settings if bit 9 is a 1
12	Enables light pen change
13	Turns the light pen on when it is a 1, or off when it is 0, provided that bit 11 is a 1
14	Enables intensity change
15,16,17	Determine one of eight possible intensity settings if bit 14 is a 1.

A.1.2 Table Control

The table control character is specified by having 101_2 in bits 6-8 of the dispatch table word. This control character has the ability to change the CASE bit and the SAR.

			Case	Enable Bits 12-14	Enable Bits 15-17	SAR (0-2)			SAR (3-5)		
6 1	7 0	8 1	9	10	11	12	13	14	15	16	17

Bits	Interpretation
6	=1 Control character
7,8	=01 Table control
9	Case bit is set by this bit for referencing, 128 characters using 6-bit code size
10	Enable changing SAR bits 6-8 from bits 12-14 of control word
11	Enable changing SAR bits 9-11 from bits 15-17 of control word
12,14	Set SAR bits 6-8 if bit 10 is a 1
15-17	Set SAR bits 9-11 if bit 11 is a 1

A.1.3 Miscellaneous Control

The miscellaneous control character is specified by 110_2 in bits 6-8 of the dispatch table word. In this format the code size can be changed, the intensity and scale can be counted up and down, and carriage return (clear low-order 10 bits of x-position register), and escape to control state (end character string, leave character generator) can be executed.

Dispatch Table Word (Miscellaneous Control)											
			CHSZ		Carriage Return	Escape	Count Scale		Count Intensity		Spare
6	7	8	9	10	11	12	13	14	15	16	17
1	1	0									

Bits	Interpretation
6	=1 Control character
7,8	=10 Miscellaneous control
9	Enable change of code size
10	Set code size to six bit, if bit is 0; set to seven bit, if bit is a 1; if bit nine is a 1
11	Clear low-order 10 bits of x-position register (carriage return) if bit is a 1
12	Escape to control state if bit is a 1
13	Enable count scale logic
14	0: count scale up 1: count scale down

Bits	Interpretation
15	Enable count intensity logic
16	0: count intensity up 1: count intensity down
17	Spare

/Program example of the use of the VC38 Character Generator.

```
INITIAL  LAC XPDP          /DISPLAY START UP
         SPDP              /SEE PROGRAMMING MANUAL
         LAC SIC
         SIC
         LAC XLBF
         LBF
         LAC XCG
         SCG
         LAC XIN
         INIT
         CLA
         ION
         JMP .
XPDP     7000
XSIC     2367
XLBF     4000
XCG      0006
XIN      DISSTT
                           /BEGINNING OF THE DISPLAY FILE
DISSTT   POINT!EDS!CCB!CBS /ENTER POINT MODE
         1000              /SET POINT TO MIDDLE OF
         5000              /THE SCREEN AND ESCAPE
         CHAR EDS          /ENTER CHARACTER MODE
         0001              /CALL CHARACTER (00) -SET SCALE AND INTENSITY
                           /THEN CHARACTER (01) - ALPHANUMERIC A
         0203              /CARRIAGE RETURN (02) - LINE FEED (03)
         0105              /ALPHANUMERIC A (01) - ESCAPE TO CONTROL STATE
                           /(04)
```

```
        JUMP            /DISPLAY JUMP TO TOP OF DISPLAY FILE
        DISSTT
        .LOC 6000
D       4555            /PARAMETER CONTROL:SC2 LPOF, INT5
        ALPA-D          /DISPATCH IN INCREMENT MODE TO ALPHA A
        6100            /MISCELLANEOUS CONTROL:  CARRIAGE RETURN
        LINFD-D+2000    /DISPATCH IN SHORT VECTOR MODE TO LINE FEED
                        /ROUTINE
        6040            /MISCELLANEOUS CONTROL:  ESCAPE TO CONTROL
                        /STATE
        .               /THE REST OF THE DISPATCH TABLE
        .LOC D+200
ALPA    1672            /ALPHANUMERIC A IN
        7251            /INCREMENT MODE:  SEE PROGRAMMING MANUAL
                        /FOR DETAILS
        6057
        7674
        3762
        2701
LINFD   3140            /SHORT VECTOR LINE FEED - (9 base 10) POINTS IN THE
                        /MINUS Y DIRECTION
ALPB    etc.            /THE REST OF THE CHARACTER ROUTINES
        .
        .
        .
        .
```

APPENDIX B

PROGRAMMING EXAMPLES

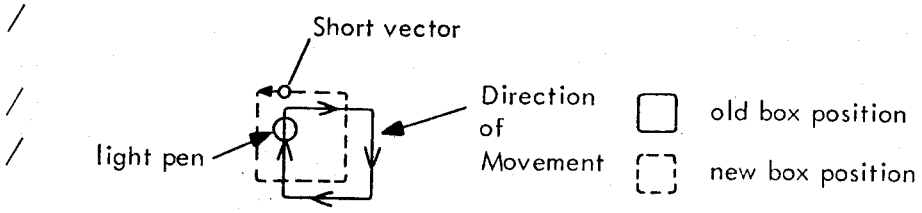
```
        /INTERRUPT HANDLER, THE DISPLAY IS
        /PLACED FIRST, HOWEVER, A DEVICE WITH CRITICAL
        /TIMING SHOULD BE BEFORE THE 339, E.G., TAPE OR DRUM.
             CLA
INTER        SPLP          /SKIP ON LIGHT PEN FLAG
             SKP
             JMP LPR       /JUMP TO LIGHT PEN ROUTINE
             SPSF          /SKIP ON INTERNAL STOP FLAG
             SKP
             JMP SFR       /JUMP TO STOP FLAG ROUTINE
             SPMI          /SKIP ON MANUAL INTERRUPT
             SKP
             JMP MIR       /JUMP TO MANUAL INTERRUPT ROUTINE
             SPEF          /SKIP ON EDGE FLAG
             SKP
             JMP EFR       /JUMP TO EDGE FLAG ROUTINE
             SPES          /SKIP ON EXTERNAL STOP FLAG
             SKP
             JMP ESR       /JUMP TO EXTERNAL STOP ROUTINE
             SPSP          /SKIP ON SLAVE LIGHT PEN ROUTINE
             SKP
             JMP SLR       /JUMP TO SLAVE LIGHT PEN ROUTINE
             RS1           /READ STATUS 1
             AND (20       /TEST BIT 13 FOR PUSHBUTTON FLAG
             SZA!CLA
             JMP PBR       /JUMP TO PUSHBUTTON ROUTINE
                           /CONTINUE CHECKING OTHER I/O EQUIPMENT
```

```
        /THE FOLLOWING DISPLAY FILE CAN BE USED
        /TO CONTROL THE SCALE, INTENSITY, AND
        /BLINK OF A PICTURE FOLLOWING THE ROUTINE.
HEADR1  SK1 40 CLAT             /SKIP 2 LOCATIONS IF PUSHBUTTON 0 IS A 0, CLEAR
                                /AFTER TEST
        SCUP                    /COUNT THE SCALE UP IF PB0 WAS 1
        0                       /NOP
        SK1!20!CLAT             /SKIP IF PB1 IS 0, CLEAR AFTER TEST
        SCDN                    /COUNT THE SCALE DOWN IF PB1 WAS 1
        0                       /NOP
        SK1!10!CLAT             /SKIP IF PB2 IS 0, CLEAR AFTER TEST
        INTUP                   /COUNT INTENSITY UP
        0                       /NOP
        SK1!4!CLAT              /SKIP IF PB3 IS 0, CLEAR AFTER TEST
        INTDN                   /COUNT INTENSITY DOWN
        0                       /NOP
        SK1!2!CLAT              /SKIP IF PB4 IS 0, CLEAR AFTER TEST
        BKON                    /TURN THE BLINK ON
        0                       /NOP
        SK1!1!CLAT              /SKIP IF PB5 IS 0, CLEAR AFTER TEST
        BKOF                    /TURN THE BLINK OFF
        0                       /NOP

        /PLACE THE REST OF THE DISPLAY
        /FILE HERE
```

```
        /THE FOLLOWING ROUTINE IS USED TO
        /TRANSLATE A PICTURE IF THE PICTURE IS
        /CLOSED IN X-Y AND CONTAINS NO POINT
        /OR GRAPHPLOT MODE INSTRUCTIONS.
HEADR2  SK2!40          /SKIP IF PB6 IS OFF
        SVEC!EDS        /SHORT VECTOR ENTER DATA STATE
        41              /ΔX=1; SHIFT PICTURE TO THE RIGHT
        SK2!20          /SKIP IF PB7 IS OFF
        SVEC!EDS
        61              /ΔX=-1; SHIFT PICTURE TO THE LEFT
        SK2!10          /SKIP IF PB8 IS OFF
        SVEC!EDS
        140             /ΔY=1; SHIFT PICTURE UP
        SK2!4           /SKIP IF PB9 IS OFF
        SVEC!EDS
        2140            /ΔY=-1; SHIFT PICTURE DOWN
        SK2!2!CLAT      /SKIP IF PB10 IS OFF; CLEAR AFTER TEST
        CCB CSB         /CLEAR COORDINATE AND SECTOR BITS
        0               /NOP
        SK2!1           /SKIP IF PB11 IS OFF
        SK2!74!CLAT     /CLEAR PB'S 6,7,8,9 IF
        0               /PB11 IS ON. CAUSES SINGLE
        0               /MOVE EACH TIME ONE OF THE BUTTONS IS PUSHED
        STOP            /STOP THE DISPLAY AND RECORD THE NEW STARTING
                        /COORDINATES
```

```
        /THIS ROUTINE PRODUCES A RASTER
        /WITH EVERY EIGHTH POINT ON THE
        /SCREEN INTENSIFIED.  THE RASTER IS
        /PUT UP IF PB5 IS ON.  THE Y OVERFLOW
        /MUST BE SET AT GREATER THAN 10 BITS
RAST    SKIP!PB5!INV        /SKIP IF PB5 IS ON
        JUMP                /JUMP OVER THE RASTER
        MAST                /ROUTINE
        SCOPE!LPON!INT 6    /SET BEAM TO LOWER LEFT CORNER
        CCB!CSB
RAS     VEC!EDS
        4001                /INTENSIFY ΔY=1
        4177                /ESCAPE ΔX=177 (ACROSS THE SCREEN AT SCALE 8)
        POINT!EDS
        2000                /DO NOT CHANGE Y COORDINATE
        4000                /ESCAPE.  SET X TO 0
        SNSZ                /HAVE WE RUN OFF THE TOP OF THE SCREEN YET?
        JUMP                /NO!.  GO BACK AND GENERATE
        RAS                 /ANOTHER LINE OF THE RASTER
        LPOF                /SHUT LIGHT PEN OFF
        VEC!EDS!CCB!CSB     /THIS VECTOR
YVECI   0                   /IS CHANGED WHEN PICTURE IS
XVECI   4000                /SHIFTED TO GET BACK TO VIRTUAL STARTING POINT.

MAST    JUMP                /CONTINUE ON
        PICT
```

```
        /PROGRAM TO KEEP BOX UNDER THE
        /LIGHT PEN, ASSUMING STARTUP IOT'S
        /WERE GIVEN AND STANDARD INTERRUPT
        /SYSTEM IS SOME PLACE IN CORE.
            CLA                     /PDP-9 GOT TO THIS LOCATION THROUGH INTERRUPT
                                    /HANDLER GIVEN ABOVE
LPR         RPB                     /READ IN CONTENTS OF 12 PUSHBUTTONS
            AND (76                 /KEEP CONTENTS OF BUTTONS 6-10 SET 11 TO 0
            TAD (300                /ADD ENABLE AND BANK BIT
            LBF                     /GIVE THE IOT TO CLEAR PB11
            CLA                     /IOT'S DO NOT CLEAR AC
            RES1                    /RESUME DISPLAY SEQUENCE AFTER LIGHT PEN HIT
            ION                     /TURN INTERRUPT SYSTEM ON
            JMP.                    /WAIT FOR NEXT PEN HIT
DISSTT      SC2!LPON!INT 6
            VEC!EDS!CSB
            4050                    /ΔY=40; INTENSIFY
            4000                    /ΔX=0; ESCAPE
            SK2!1! INV!CLAT!COAT
            SVEC!EDS
            61                      /ΔY=0, ΔX=-1; ESCAPE
            VEC!EDS
            4000                    /ΔY=0; INTENSIFY
            4050                    /ΔX=40; ESCAPE
            SK2!1!INV!CLAT!COAT
            SVEC!EDS
            140                     /ΔY=1, ΔX=0; ESCAPE
            VEC!EDS
            6050                    /ΔY=-40; INTENSIFY
            4000                    /ΔX=0; ESCAPE
            SK2!1!INV!CLAT!COAT
            SVEC!EDS
            41                      /ΔY=0, ΔX=1; ESCAPE
            VEC!EDS
            4000                    /ΔY=0; INTENSIFY
            6050                    /ΔX=-40; ESCAPE
            SK2!1!INV!CLAT!COAT
            SVEC!EDS
            2140                    /ΔY=-1. ΔX=0; ESCAPE
            JUMP
            DISSTT
        /PROGRAM WORKS AS FOLLOWS:
        /PUSHBUTTON 11 IS SENSED AT THE END OF
        /EACH SIDE. IF THE BUTTON IS ON, THE
        /NEXT SIDE IS DRAWN, IF THE BUTTON IS
        /OFF, A SHORT INVISIBLE VECTOR IS EXECUTED
        /IN THE PROPER DIRECTION TO KEEP THE BOX
        /UNDER THE PEN
```




```
/THE BUTTON IS TURNED BACK ON
/THEN THE NEXT SIDE IS DRAWN.
```

APPENDIX C
REFERENCE TABLES

Table C-1
Control State Summary

Op Code: Parameter			Scale			Light Pen		Intensity			
6	7	8	9	10	11	12	13	14	15	16	17
0	0	0									

Op Code: Mode			Stop Code	Clear Push-Button Flag	Mode			Clear Sector Bits	Clear Coord-inate Bits	Enter Data State
6	7	8	9	10	11	12	13	14	15	16	17
0	0	1									

First Word

Op Code: Jump			Scale			Light Pen		Push	Break Field		
6	7	8	9	10	11	12	13	14	15	16	17
0	1	0									

Second Word

Low Order 12 Bits of Address											
6	7	8	9	10	11	12	13	14	15	16	17

								Inhibit Restoring			
Op Code: Pop			Scale			Light Pen		Mode	Light Pen and Scale	Intensity	Enter Data State
6	7	8	9	10	11	12	13	14	15	16	17

Op Code: Conditional Skip (Bank 1)			Sense of Test	Clear Bits After Test	Comple-ment Bits After Test	Selected Pushbuttons 0-5					
						PB0	PB1	PB2	PB3	PB4	PB5
6	7	8	9	10	11	12	13	14	15	16	17
1	0	0									

Table C-1 (Cont)
Control State Summary

Op Code: Conditional Skip (Bank 2)			Sense of Test	Clear Bits After Test	Complements Bits After Test	Selected Pushbuttons 6-11					
						PB6	PB7	PB8	PB9	PB10	PB11
6 1	7 0	8 1	9	10	11	12	13	14	15	16	17

Op Code: Miscellaneous			Microprogrammed: Arithmetic Compare PB (0-5)			Pushbuttons (0-5)					
						PB0	PB1	PB2	PB3	PB4	PB5
6 1	7 1	8 0	9 0	10 0	11 0	12	13	14	15	16	17

Op Code: Miscellaneous			Microprogrammed: Arithmetic Compare PB (6-11)			Pushbuttons (6-11)					
						PB6	PB7	PB8	PB9	PB10	PB11
6 1	7 1	8 0	9 0	10 0	11 1	12	13	14	15	16	17

Op Code: Miscellaneous			Microprogrammed: Skip on Flags			Skip Unconditional	Skip if not Sector 0	Skip on Pushbutton Hit Flag		Skip on	Clear
								Bank 1	Bank 2	LPSI	LPSI
6 1	7 1	8 0	9 0	10 1	11 0	12	13	14	15	16	17

Op Code: Miscellaneous			Microprogrammed: Count			Count Scale		Count Intensity		Blink	
										On	Off
6 1	7 1	8 0	9 0	10 1	11 1	12	13	14	15	16	17

Op Code: Miscellaneous			Micro-pro: Slaves	Group Number		Unit 0			Unit 1		
6 1	7 1	8 0	9 1	10	11	12	13	14	15	16	17

Table C-2
Data State Summary

First Word (ΔY)

Point (000)											
Intensify	Inhibit	Y Position									
6	7	8	9	10	11	12	13	14	15	16	17

Second Word (ΔX)

Point (000)											
Escape	Inhibit	X Position									
6	7	8	9	10	11	12	13	14	15	16	17

Increment 001											
Intensify	No. of Moves		Direction (0-7)			Intensify	No. of Moves		Direction (0-7)		
6	7	8	9	10	11	12	13	14	15	16	17

First Word (ΔY)

Vector (010)											
Intensify	+ −	10-Bit ΔY									
6	7	8	9	10	11	12	13	14	15	16	17

Second Word (ΔX)

Vector (010)											
Escape	+ −	10-Bit ΔX									
6	7	8	9	10	11	12	13	14	15	16	17

Table C-2 (Cont)
Data State Summary

Vector Continue (011)											
Intensify	+ −	10-Bit ΔY									
6	7	8	9	10	11	12	13	14	15	16	17
Escape		10-Bit ΔX									
6	7	8	9	10	11	12	13	14	15	16	17

Short Vector (100)											
Intensify	+ −	ΔY				Escape	+ −	ΔX			
6	7	8	9	10	11	12	13	14	15	16	17

Six-Bit Format

Character (101)											
Character 1						Character 2					
6	7	8	9	10	11	12	13	14	15	16	17

Seven-Bit Format

Ignored					Character						
6	7	8	9	10	11	12	13	14	15	16	17

Graphplot (110)											
Escape	Set Y Set X	X or Y Coordinate									
6	7	8	9	10	11	12	13	14	15	16	17

Table C-3

Mnemonic Summary

Mnemonic Symbol	Octal Code	Operation
LPOF	0040	Light pen off
LPON	0060	Light pen on
SC1	0400	Set scale to X1
SC2	0500	Set scale to X2
SC4	0600	Set scale to X4
SC8	0700	Set scale to X8
INT*	0010	Set the intensity
EDS	1001	Enter data state
CCB	1002	Clear coordinate bits
CSB	1004	Clear sector bits
POINT	1100	Set mode to 0
INCR	1110	Set mode to 1
VEC	1120	Set mode to 2
VECON	1130	Set mode to 3
SVEC	1140	Set mode to 4
CHAR 5	1150	Set mode to 5
GRAPH	1160	Set mode to 6
CHAR 6	1170	Set mode to 7
CLDF	1200	Clear flag. Pushbutton hit flag
STOP	1400	Stop display
JUMP	2000	Jump to 15-bit address contained in last digit and the next word addressed
PJMP	2010	Jump to subroutine addressed the same as JUMP
POP	3000	Exit from subroutine to next address after PJMP
PEDS	3001	Pop and enter data state
PNI	3002	Pop and inhibit restoring intensity
PNLS	3004	Pop and inhibit restoring light pen and scale
PNM	3010	Pop and inhibit restoring mode
SK1	4000	Skip if any of the selected pushbuttons are 0
INV	0400	Invert sense of test (skip if any selected pushbutton is 1)
CLAT	0200	Clear buttons tested after test

Table C-3 (Contd)

Mnemonic Summary

Mnemonic Symbol	Octal Code	Operation
COAT	0100	Complement buttons tested after test
SK2	5000	Skip if any of the selected pushbuttons are 0
SK3	6000	Arithmetically compare pushbuttons (0-5) with last two digits of instruction; skip if not equal
SK4	6100	Same as SK3 but for pushbuttons 6-11
SKIP	6240	Unconditional skip (two locations)
SNSZ	6220	Skip if sector 0 flag is not up
SPB1	6210	Skip if pushbutton (0-5) flag is down
SPB2	6204	Skip if pushbutton (6-11) flag is down
SLPSI	6202	Skip on not LPSI
CLPSI	6201	Clear LPSI
SCUP	6340	Count scale up
SCDN	6360	Count scale down
INTUP	6310	Count intensity up
INTDN	6314	Count intensity down
BKON	6302	Blink on
BKOF	6301	Blink off
SG0	6400	Set slave group 0
SG1	6500	Set slave group 1
SG2	6600	Set slave group 2
SG3	6700	Set slave group 3
SU0	0040	Turn light pen and intensity off on unit 0
LP0	0060	Unit 0 light pen on
IT0	0050	Unit 0 intensity on
SU1	0004	Turn light pen and intensity off on unit 1
LP1	0006	Unit 1 light pen on
IT1	0005	Unit 1 intensity on

Table C-4

IOT Summary

IOT	Octal Code	Definition
RPDP	700501	Read Puchdown Pointer
RXP	700502	Read X-Position Register Bits 1-12
RYP	701602	Read Y-Position Register Bits 1-12
RDAC	700601	Read Display Address Counter
RS1	700602	Read Status 1
RS2	701622	Read Status 2
RS3 RPB	700621	Read Pushbuttons
RS4 RSG1	700622	Read Slave Group 1
RS5 RSG2	701642	Read Slave Group 2
SPDP	700645	Set the Pushdown Pointer
SIC	700665	Set Initial Conditions
LBF	700705	Load Break Field
SCG	700743	Set Character Generator
INIT	701605	Initialize the Display
RES1	700724	Resume After Light Pen Hit Edge on External Stop
RES2	701604	Resume After Stop Code
CFD	701601	Clean Display Flags
STPD	700704	Stop Display (External)
SPLP	700642	Skip on Light Pen Hit Flag
SPSP	700662	Skip on Slave Light Pen Hit Flag
SPES	700701	Skip on External Stop Flag
SPEF	700702	Skip on Edge Flag
SPSF	700721	Skip on Internal Stop Flag
SPMI	700722	Skip on Manual Interrupt
RCG	701662	Read Character Generator
SPDF	700761	Skip on Data Flag (used with VF38 Search Option)
SPPF	700762	Skip on Pop Flag (used with VF38 Search Option)
SIVF	700764	Set INMS on VRS Flags (used with VF38 Search Option)

Table C-5
Status Format

RS1

L.P. Hit Flag	Vertical Edge Flag	Hori-zontal Edge Flag	Internal Stop Flag	Sector Zero Flag	Control State Flag	Manual Inter-rupt Flag	P.B. Hit Flag	Display Inter-rupt Flag	Break Field		
6	7	8	9	10	11	12	13	14	15	16	17

RS2

Byte	L.P. Enable	Y Position Bit 0	X Position Bit 0	Scale		Mode			Intensity		
6	7	8	9	10	11	12	13	14	15	16	17

RCG

Char-acter	CB	Spare	Case	CHSZ	Spare	SAR					
6	7	8	9	10	11	12	13	14	15	16	17

SIC

Edge Inter-rupt	L.P. Inter-rupt	L.P. Resume Options		Y Dimension		X Dimension		Intensify All Points	Inhibit Edge Flags	P.B. Inter-rupt	Internal Stop Inter-rupt
6	7	8	9	10	11	12	13	14	15	16	17

LBF

Break Field				Pushbuttons							
6	7	8	9	10	11	12	13	14	15	16	17

SCG

Spare			Case	CHSZ	Spare	SAR					
6	7	8	9	10	11	12	13	14	15	16	17